Low-temperature thermal oxide to Plasma-Enhanced Chemical Vapor Deposition oxide wafer bonding for thin-film transfer application

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Abstract: Low-temperature direct Plasma-Enhanced Chemical Vapor Deposition (PECVD) oxide to thermal oxide bonding is described. The PECVD oxide is densified at 350°C and chemical-mechanically polished to obtain reasonably smooth surface for bonding. The PECVD oxide wafer is bonded to the thermal oxide wafer at room temperature after piranha clean that leaves the wafer surfaces hydrophilic. A post-bonding anneal at 300°C completes the bonding. A void-free bonding interface is observed from infrared imaging and the bonding strength is estimated to be 432 mJ/m^2. This bonding method can be used in a variety of applications, including three-dimensional integration.

Three-dimensional (3-D) integration, in the form of a vertical stack of several device (with interconnect) layers, has many potential advantages over conventional horizontal planar integration [1]. There are research efforts on developing possible technology options to realize a 3-D structure, either using recrystallization [2,3] or wafer bonding [4,5]. We have recently proposed a 3-D integration method using direct Cu-to-Cu wafer bonding [6]. In this scheme, a thinned silicon-on-insulator (SOI) device layer is bonded to a substrate device wafer in a back-to-face fashion. This requires bonding of the SOI wafer to a handle wafer followed by SOI wafer etchback. The thinned SOI layer is then bonded to the substrate device wafer using Cu as the bonding medium. Note that the bonding between the SOI wafer and the handle wafer is a sacrificial one, as the handle wafer will be released at the end of the process. Hence, this bond has to be strong enough to hold the SOI wafers during subsequent processes. However, the same bonding should release readily during SOI thin-film transfer onto the substrate wafer. Epoxy [7] and adhesive [8] have been investigated, but they are not compatible with the process temperature during Cu wafer bonding at 400°C and the chemical attack during SOI wafer etchback. In this letter, we describe a direct thermal oxide to Plasma-Enhanced Chemical Vapor Deposition (PECVD) oxide wafer bonding for this application. The choice of two different oxides will be explained below.

All wafers used in our experiment were *p*-type 4" Si(100) wafers of 10-20 Ω-cm resistivity. Two sets of wafers were prepared: One was the handle wafers and the other was the dummy SOI wafers. The handle wafers were covered with 5000Å of thermal oxide for protection against chemical attack during SOI wafers etchback. Wet silicon etchants such as KOH and TMAH are known to have excellent selectivity towards

thermal oxide [9]. Dummy SOI structures were prepared by growing 5000Å of thermal oxide as buried oxide (BOX) followed by a deposition of 4000 Å undoped polysilicon at 620°C. The SOI wafers were then coated with 4μm of silane-based PECVD oxide at 400°C. In actual device wafers with metal interconnects, PECVD oxide is an attractive choice as interlayer dielectric (ILD) because of its high deposition rate and its low temperature process. However, due to the non-equilibrium nature of the PECVD process, byproducts or gas molecules may be incorporated into the deposited film and result in out-gassing during subsequent processing [10]. To prevent undesired out-gassing from the PECVD oxide film during subsequent heat treatment of the bonded wafer pairs, the SOI wafers were densified in atmospheric N_2 ambient at 350 ^{o}C for 16 hours.

Since as-deposited PECVD oxide exhibits a relatively high surface roughness, direct bonding using such wafers are often unsuccessful. Therefore, the SOI wafers were chemical-mechanically polished after densification to increase both the surface smoothness and the bonding yield. To ensure that this bonding method is useful in real device wafers, a low temperature process is essential to avoid undesired thermal damage. Hence, a hydrophilic bonding was chosen. All wafers received a 10 min piranha (H_2O_2 : H_2SO_4 = 1:3) solution clean followed by deionized water rinse and spin-dry. This cleaning was necessary to clean the polished wafers and to terminate the wafer surfaces with hydroxyl (OH) groups to initiate wafer bonding. Handle wafers were aligned to SOI wafers in an EV1 aligner and the pairs were subsequently transferred to a bonder. The chamber was purged with nitrogen and evacuated to 10^{-3} Torr. Bonding occurred at room temperature under a pressure of 1000 mbar for 5 min. Figure 1 is a schematic showing

the bonding process. After bonding, the wafer pairs were annealed at 200 ^{o}C and 300 ^{o}C respectively for 6 hours in atmospheric N_2 ambient to enhance the bonding strength.

To achieve high quality bonding, the root-mean-square (RMS) roughness of the wafers must be below 1.0 nm [11]. Atomic force microscopy (AFM) is a powerful tool to scan the surface profile and to measure the roughness of different materials. We have performed AFM surface scans on various wafers in the tapping mode on a D3000 unit from Digital Instruments. Table I summarizes the mean and RMS roughness of various wafers with different surface preparations. The handle wafers with a layer of 5000 Å of thermal oxide exhibit an RMS roughness of 0.273 nm, and this value is acceptable for bonding. Hence the handle wafers do not require additional surface polishing.

On the other hand, the RMS roughness of the as-deposited PECVD oxide on SOI dummy wafers is 9.757 nm. This value is too high for wafer bonding and the wafers need extra polishing to smoothen their surfaces. We have also monitored the change in the surface roughness of the PECVD oxide as a result of densification. It was observed that densification has improved the roughness to 8.501 nm. This suggests that densification anneal has effectively improved the structure of the PECVD oxide. Figure 2 shows the RMS roughness of the PECVD oxide as function of chemical-mechanical polishing (CMP) duration. Note that CMP has improved the surface roughness tremendously to a value below 1.0 nm after one minute of polishing and the roughness does not improve significantly beyond one minute. Specifically, a 3 min CMP results in a roughness of 0.394 nm. In the bonding experiment, we have used 3 min of CMP on all PECVD oxide wafers unless otherwise specified.

When two wafers are brought into contact at room temperature, hydrogen bonds between hydroxyl (OH) groups are established across the gap between the wafers. The strength of the hydrogen bonds will decrease sharply as the distance between the OH groups increases. Since there is less intimate contact area when the wafers surface is rough, the number of strong bond will be limited and the bond strength will decrease. Figure 3 compares the 3μm x 3μm surface profiles of the as-deposited PECVD oxide and PECVD oxide that has undergone 16 hours of N_2 anneal at 350°C and 3 min of CMP. Note the obvious difference between the two wafers in terms of surface profile. The uneven surface profile of the as-deposited oxide film will limit the amount of surface area that can be in intimate contact with its pairing wafer, which in turn will degrade the quality of the bonding. The densified and polished wafer, on the other hand, is much more even and will promote better wafer bonding. Therefore, CMP is an effective tool to achieve reasonable surface smoothness for PECVD oxide wafer bonding.

Since hydrogen bonds between the bonded wafer pair are relatively weak, a heat treatment can be used to strengthen the bond. In this section, we will study the effect of post-bonding anneal on the bonding strength. For the purpose of our application, we have limited the anneal temperature to 300°C. We have used the Maszara's crack opening method to quantify the bond strength. In this method, a razor blade of thickness $2y$ is inserted into the edge of the bonded wafer pair and the crack length L is measured from the infrared (IR) image. The bonding strength, given by the average surface energy of the bonded pair γ in J/m^2, can be estimated from the following relation [12]:

$$\gamma = \frac{3Et^3y^2}{8L^4} \quad (1)$$

where E = 166 GPa, the modulus of elasticity for Si(100), $2y$ and L are the crack separation and length, respectively, and t is the thickness of the wafer. Note that we have neglected the presence of oxide due to its much smaller thickness compared to the wafer thickness. We have performed the crack opening experiment at a temperature of 23°C and relative humidity of 28%.

Figure 4 shows how bond strength evolves as a function of post-bonding anneal temperature. The bonding strength is only 170 mJ/m^2 after room temperature bonding and increases to 298 mJ/m^2 after a 6 hours anneal at 200°C. At 200°C, the OH groups gain more surface mobility and more hydrogen bonds develop across the gap [12]. The reaction of surface silanol (Si-OH) groups also takes place during post bonding annealing:

$$\text{Si-OH} + \text{OH-Si} \rightarrow \text{Si-O-Si} + H_2O \quad (2)$$

The bonding strength is 432 mJ/m^2 after a 6 hours anneal at 300°C. This is because at higher temperature, reaction (2) is promoted and the water molecules gain more surface mobility and diffuse out of the bonding interface. As a result, the strong siloxane (Si-O-Si) bonds are formed. This shows that post-bonding anneal is useful in enhancing the bonding strength.

During wafer bonding, trapped air bubbles can cause undesired interface voids and this will affect the interface quality of the bonded wafer pair. Infrared imaging is a convenient and common way to examine the interface voids of the bonded wafer pairs. Since both silicon (E_g = 1.12 eV) and SiO_2 (E_g = 8.0 eV) are transparent to infrared, interface voids can be viewed by transmitting infrared light through one side of the bonded wafer pair. An infrared camera can then be used to detect the interface void at the

other side of the bonded wafer pair. Besides infrared imaging, scanning acoustic microscopy and X-ray topography can also be used to examine interface voids.

Figure 5 shows IR images from the bonded wafer pairs before and after post-bonding anneal. Figures 5(a) and 5(b) are the IR images for wafer pair without pre-bonding densification of the PECVD oxide. It is evident that voids form in this wafer pair. The voids form possibly due to out-gassing from the undensified PECVD oxide during post-bonding anneal. However, the wafer pair with densified PECVD oxide bonds very well and no observable void is found from the IR images. The IR images for this wafer pair before and after post-bonding densification are shown in Figs. 5(c) and 5(d) respectively. This suggests the importance of densification for successful bonding.

We concluded that low temperature bonding of PECVD oxide to thermal oxide is achievable with proper surface preparations. To ensure successful bonding, the PECVD oxide needs to be densified to prevent out-gassing and polished to smoothen its surface. The bonding strength of the wafer pair bonded at room temperature can be further improved by post-bonding anneal. This bonding method may find application in 3-D technologies, such as in thin-film transfer based on Cu wafer bonding.

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TABLES

Table I. Mean and RMS roughness of wafers with different surface preparations estimated from AFM.

Wafer Description	Mean Roughness (nm)	RMS Roughness (nm)
Bare Si wafer	0.097	0.143
5000Å SiO_2/Si	0.202	0.273
4µm PECVD SiO_2/SOI (As prepared)	7.929	9.757
4µm PECVD SiO_2/SOI (Annealed at 350°C for16 hrs)	6.877	8.501
4µm PECVD SiO_2/SOI (Annealed at 350°C for16 hrs + 3min CPM)	0.312	0.394

FIGURE CAPTIONS

Figure 1. Schematic shows the bonding of thermal oxide on a handle wafer to PECVD oxide on an SOI structure.

Figure 2. RMS roughness of PECVD oxide as a function of CMP duration. Note that the roughness falls below 1.0 nm and does not change significantly beyond 1 minute.

Figure 3. AFM scans for (a) as-deposited PECVD oxide, and (b) densified and polished PECVD oxide.

Figure 4. Bonding strength of the bonded wafer pairs with different post-bonding heat treatments.

Figure 5. The effect of post-bonding annealing on bonding interface for: (a)-(b) wafer pair without densification on PECVD oxide, and (c)-(d) wafer pair with densification on PECVD oxide. (a) and (c) are IR images before annealing, and (b) and (d) are IR images after annealing.

FIGURES

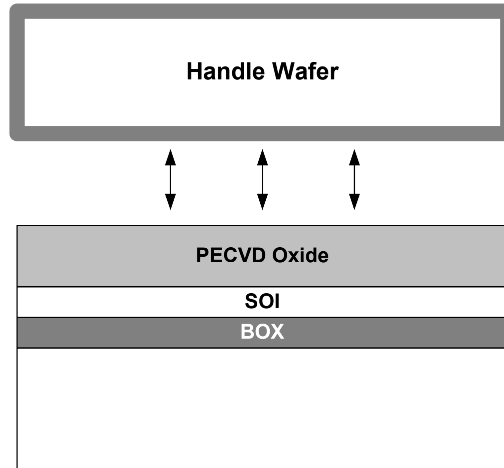

Figure 1

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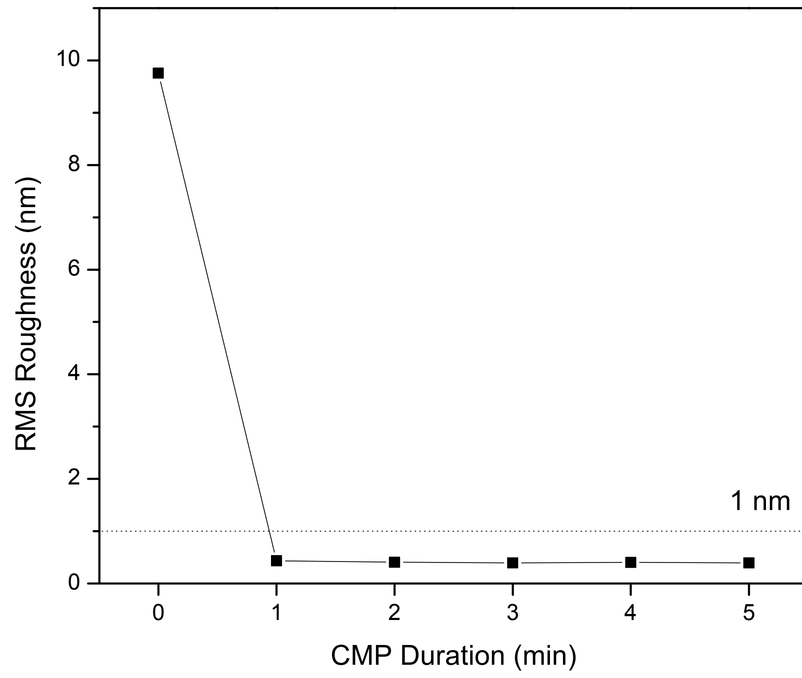

Figure 2

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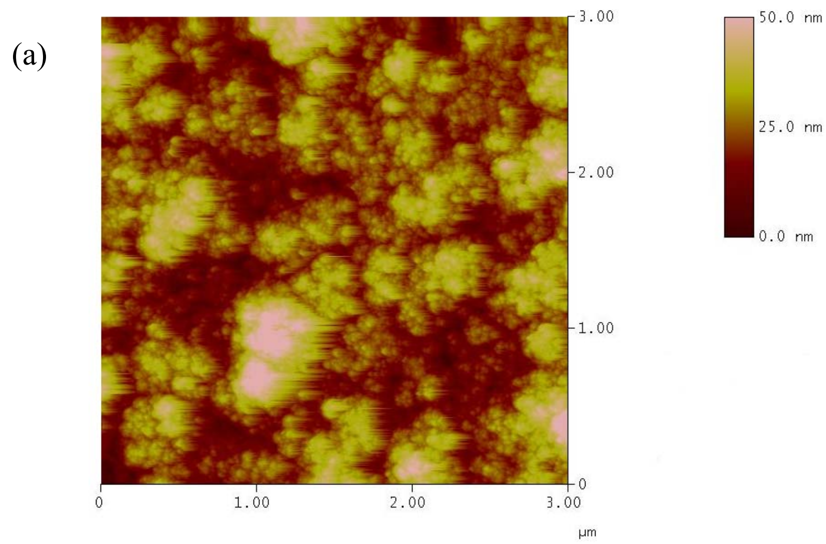
(a)



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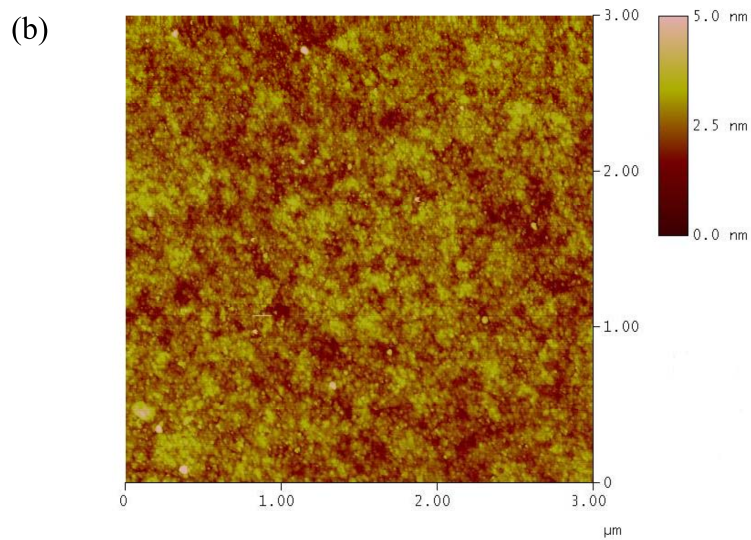

Figure 3

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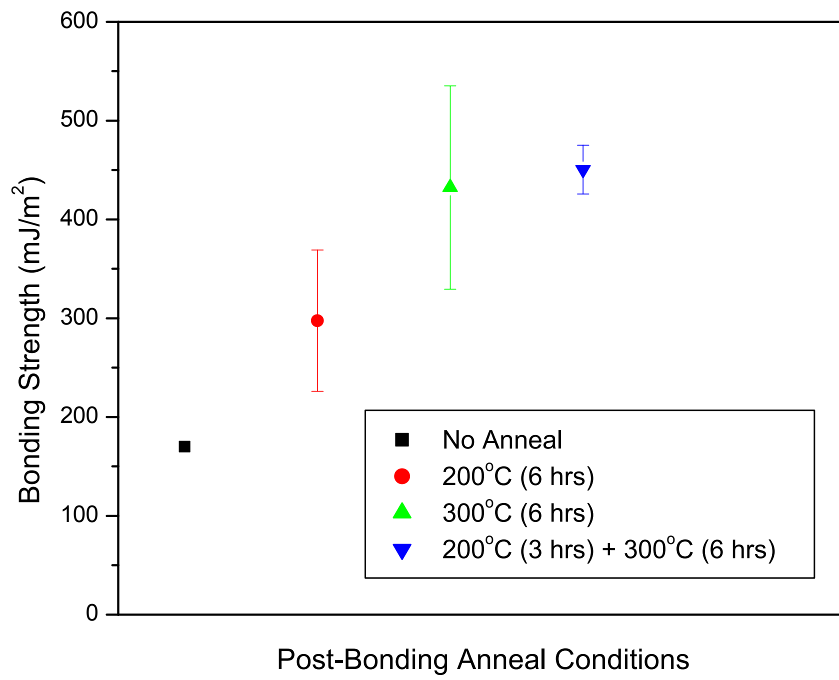

Figure 4

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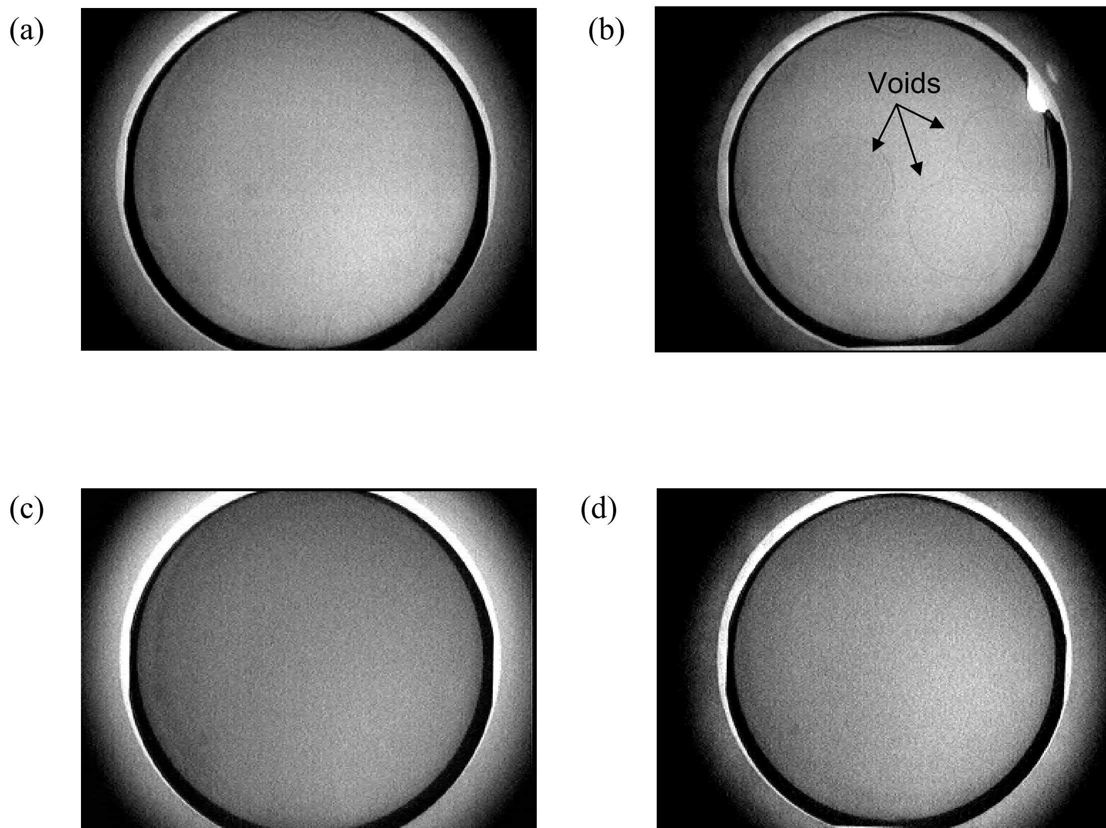

Figure 5

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