An alternative technique for digitizing charge signals, charge-to-digital conversion, is free from many difficulties with conventional methods. Its advantages occur because A/D conversion is performed in the charge, rather than the voltage, domain. Digitizing charge quanta is conventionally performed by a multistage procedure such as that shown in Figure 1a. A charge packet is first dumped onto a preset capacitor whose voltage falls in response. The resulting pulse is buffered, driven off-chip, and amplified. The signal is then sampled and processed to reduce noise. Finally, the resulting voltage is digitized by an A/D converter. This process translates a charge packet to an intermediate clocked voltage waveform, that must then be resampled. These operations constitute a majority of the hardware, power, and complexity required for readout and each introduce noise and nonlinearity.

Digitization may be consolidated by digitizing charge signals on-chip, in the charge domain. In this method, charge packets are transferred directly into a charge-to-digital converter (CDC), implemented using CCD elements (Figure 1b). Signals continue as discrete-time charge quanta throughout conversion and no charge-to-voltage translation or resampling occurs.

Two CCD-based A/D converters previously reported have approximately 4b performance [1, 2]. Their accuracy is limited by two factors. First, they are oriented toward a CMOS implementation and require operations, such as subtraction, not accurately achieved using CCDs. Second, their charge sensing and comparators rely on accurate charge-to-voltage translations. An architecture described in Reference 3 overcomes the need for subtraction, but faces other limitations caused by asymmetrical comparator placement and common-mode accumulation that amplifies channel mismatches and saturates sensing.

The CDC described here is based on a fully-differential, bit-serial, successive approximation architecture, shown in Figure 2, specifically tailored to CCD implementation and to the pipelined nature of CCD operations. An 8-bit converter contains a pipeline of N identical conversion blocks, through which a digital result is determined successively, from the MSB to the LSB, in a bit-serial manner. One digital word is completed each clock cycle. The pipeline is symmetrically divided into positive and negative halves. Each half consists of two charge-flow channels, referred to as accumulator and scaling channels, that pass through all blocks in the pipeline.

A single conversion block shown in Figure 3. Delay, summation, division, and conditional transfer in the figure are implemented using CCD gates. The first block accepts the differential signals to be digitized, +e and -e, into two accumulator channels and identical full-scale references, +g and -g, into two scaling channels. The accumulator charges are compared and the resulting bit is latched. At the same time, each scaling charge is divided into half. The comparator result is used to conditionally add this half to its associated accumulator in the channel that contains the least charge. All resulting signals are then passed forward so that the same process may be repeated in each successive block. The converter offset is formed from the comparator outputs generated in each stage.

The CDC may be operated with other input configurations. The negative accumulator input may remain constant for single-ended operation or may be varied each cycle to accomplish adaptive offset adjustment. The scaling inputs may be varied to achieve adaptive dynamic range adjustment, calibration, or a piecewise linear or companding conversion characteristic.

This CDC architecture requires only sampling, shifting, addition, and division by two, that are easily and accurately implemented using CCD elements. Subtraction is accomplished by complementary addition. Shifting, addition and division may be accomplished by fully-depleted charge transfers because connections exist only between neighboring elements. Comparator performance is improved by the symmetrical device structure because imbalances are minimized and sensed signals do not require buffering.

Charge-mode processing improves comparator resolution, suppresses channel mismatches, and avoids saturation [4]. This is accomplished by a differential charge replicator sensing circuit (Figure 4). The approach is based on the fact that common-mode accumulation of charge is not a problem until it is sensed as a voltage, when it occupies dynamic range and requires translation. Differential replicators operate autozeroed to amplify the differential signal and to suppress the common-mode signal before charge-to-voltage translation. Charge received by the output well, G7, is sensed by its overlying gate and is fed back to gate G5 in the opposite channel. As more charge is produced by one channel, more charge is blocked from the other.

A summary of prototype performance is given in Table 1. Although charge-to-digital conversion is primarily intended for charge quantity signals, to facilitate testing and characterization, the prototypes accept voltage inputs by an initial voltage-to-charge translation stage. Both devices are controlled by 4 external 0 to 5V clocks.

The first prototype, CDC1, includes 8 conversion blocks (Figure 7). The focus of this design was on resolution, and no emphasis was placed on optimizing its speed or power. It is implemented in a CCD/CMOS process using 2.0μm design rules. Figure 5 shows CDC1 measured spectral response to a 0.5MHz sinusoidal input as a 2MHz sampling rate. The ratio of fundamental to largest harmonic spur, or the SFDR, is 56dB. Figure 6 shows the measured effective bits, or SNDR, as a function of input power under the same operating conditions. At low frequencies CDC1 performance is limited by the initial charge generation stage and by comparator errors, while at higher frequencies charge splitting errors contribute as well. Charge transfer inefficiency was determined to be an insignificant source of error.

The focus of the second prototype, CDC2, is on high speed and low power, and less emphasis is placed on optimizing its resolution. Power dissipation for this device, including that for on-chip CCD clock generator circuits, is 13mW for 4V operation at its maximum sampling rate of 32MHz. The CDC2 is implemented in a 1.2μm, double-poly CMOS process with no special CCD provisions, and limited by dynamic comparator inaccuracies.

*This work was supported in part by the Department of the Air Force and by a National Science Foundation Graduate Fellowship.
Figure 1: Comparison of charge digitization. 
(a) Conventional. 
(b) Direct charge-to-digital conversion.

Figure 2: Pipelined Nb CDC block diagram.

Figure 3: Conversion block contents at position m.

Figure 4: Differential charge sensing and replication circuit.

Figure 5: Measured spectral response (0.5MHz sinusoidal input).

Figure 6: Measured effective bits or SNDR (2MHz sampling rate).

Figure 7: Acknowledgments and References: See page 442.

Table 1: Performance of CDC1 and CDC2 prototypes.

<table>
<thead>
<tr>
<th></th>
<th>CDC1 device</th>
<th>CDC2 device</th>
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Acknowledgments:

The authors thank A. Horst and S. Broadsone for help in device testing and Mentor Graphics Corp. for electronic design software.

References:


Figure 7: 9-stage CDC1 prototype chip micrograph.

Figure 8: VGA and SXGA image photographs.