Performance Analysis of Ultra-Scaled InAs HEMTs

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Motivation: Towards III-V MOSFET

- Strained channel
- New gate dielectrics
- Device geometries
- Channel materials
- High-k dielectrics

2015-2019 Research

III-V channel devices

Low-power & high-speed

Acknowledgement: Robert Chau, Intel
Motivation: Why III-V HEMTs?

- **III-V**: Extraordinary electron transport properties
- **HEMTs**: Very similar structure to MOSFETs except high-κ dielectric layer
- **Excellent to Test Performances** of III-V material without interface defects
- **Excellent to Test Simulation Models**
  - Develop simulation tools and benchmark with experiments
  - Predict performance of ultra-scaled devices

2007: 40nm

2008: 30nm

D.H. Kim et al., *EDL* 29, 830 (2008)
Outline

- Motivation
- Modeling Approach
  - Real-space EM simulator including gate leakage
  - Atomistic tight-binding $m^*$
  - Realistic description of simulation domain (gate geometry)
- Comparison to Experiments $L_g=30, 40, 50\text{nm}$
  - Material parameters, $I_d-V_{gs}, I_d-V_{ds}$
- Scaling Considerations for $L_g=20\text{nm}$
  - Channel thickness, Insulator thickness, Gate metal work function
- HEMT Simulator on nanoHUB.org
- Conclusion and Outlook
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Device Geometry and Simulation Domain

- **Intrinsic device**
  - Near gate contact
  - Self consistent 2D Schrodinger-Poisson
  - Electrons injected from all contacts


- **Extrinsic source/drain contacts**
  - Series resistances $R_S$ and $R_D$

Gate Geometry and Gate Leakage Current

1) Include series resistances
\[ V_{gs}^{ext} = V_{gs}^{int} + I_d R_s \]
\[ V_{ds}^{ext} = V_{ds}^{int} + I_d (R_s + R_d) \]

2) Include gate leakage current
\[ (E-H-\Sigma_s-\Sigma_D-\Sigma^G)\cdot C = (S^s + S^D + S^G) \]

3) Include the proper gate geometry flat (a) or curved (b)

Gate leakage reduced in curved gate device
Accurate Effective Mass Calculation

**Full-Band Transport:**
- Strain, Disorder, Non-parabolicity, BTBT
- No gate leakage, Computationally very intensive

**Effective Mass Transport:**
- Gate leakage, Computationally efficient
- Parabolic bands, No disorder, Wrong quantization levels

Import $m^*$

![Diagram](image.png)

- InGaAs (2nm) InAlAs (11nm)
- InAs (5nm)
- Electronic domain
- InGaAs (3nm)
- InAlAs (40nm)
- Strain domain

$\sim 4$ nm

$L_x = L_z = 3.5$ nm
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### Transfer Characteristics: $I_d - V_{gs}$

#### Parameter

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Initial</th>
<th>Final parameter set</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>30</td>
</tr>
<tr>
<td></td>
<td></td>
<td>40</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50</td>
</tr>
<tr>
<td>$L_g$ [nm]</td>
<td>30, 40, 50</td>
<td>34.0</td>
</tr>
<tr>
<td></td>
<td></td>
<td>42.0</td>
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<tr>
<td></td>
<td></td>
<td>51.25</td>
</tr>
<tr>
<td>$t_{ins}$ [nm]</td>
<td>4</td>
<td>3.6</td>
</tr>
<tr>
<td></td>
<td></td>
<td>3.8</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.0</td>
</tr>
<tr>
<td>$\Phi_M$ [eV]</td>
<td>4.7</td>
<td>4.66</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.69</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.68</td>
</tr>
<tr>
<td>$m^*_\text{ins (InAlAs)}$</td>
<td>0.075</td>
<td>0.0783</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.0783</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.0783</td>
</tr>
<tr>
<td>$m^*_\text{buf (InGaAs)}$</td>
<td>0.041</td>
<td>0.0430</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.0430</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.0430</td>
</tr>
</tbody>
</table>
Conclusion:
- Good agreement for all $L_g$’s
- Less ballistic at $L_g=50\text{nm}$
- Use models and material parameters to design ultra-scaled devices ($L_g=20\text{nm}$)
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- **Scaling Considerations for $L_g=20\text{nm}$**
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What can be changed?

- Gate geometry
- Channel thickness scaling: $t_{\text{InAs}}$
- Insulator thickness scaling: $t_{\text{ins}}$
- Metal work function engineering: $\Phi_M$

Better control of surface potential
Gate leakage reduction and E-mode operation

$L_g = 20\text{nm}$
InAs (Channel) Layer Thickness

**InAs Channel Scaling:**
- Better electrostatic control
  - lower SS
  - larger $I_{ON}/I_{OFF}$ ratio
- Increase of transport $m^*$
  - reduced $v_{inj}$, higher $N_{inv}$
  => higher $I_{ON}$
- Increase of gate leakage current
  - $I_{ON}/I_{OFF}$ ratio saturates
InAlAs (Insulator) Layer Thickness

InAlAs Insulator Scaling:

- Better electrostatic control (due to larger $C_{ox}$)
- Increase of gate leakage current
  - larger $I_{OFF}$
  - larger SS
  - smaller $I_{ON}/I_{OFF}$ ratio
**Work Function Engineering**

**Work Function Increase:**
- Shift towards enhancement mode
- Decrease of gate leakage current
- Allows for thinner insulator layer
  - steeper SS
  - larger $I_{ON}/I_{OFF}$ ratio

![Graphs showing work function engineering](image)

- $I_d \& I_g$ vs. $V_{gs}$ [V]
  - $V_{ds} = 0.50V$ (solid line), $V_{ds} = 0.05V$ (dotted line)
  - $\Phi_M = 4.7$ eV
  - $\Phi_M = 5.1$ eV

- SS vs. $t_{ins}$ [nm]
  - $\Phi_M = 4.7$ eV
  - $\Phi_M = 5.1$ eV

- $I_{ON}/I_{OFF}$ vs. $t_{ins}$ [nm]
  - $\Phi_M = 5.1$ eV
  - $\Phi_M = 4.7$ eV
### Parameters and Performances Summary

<table>
<thead>
<tr>
<th>Parameters</th>
<th>(1) Gate geometry</th>
<th>(2) Channel thickness</th>
<th>(3) Insulator thickness</th>
<th>(4) Metal work function</th>
</tr>
</thead>
</table>

- **Improved gate control**
- **Higher gate leakage**
- **Gate leakage reduction**

**InGaAs**

- InAs
- InAlAs

**Diagrams**:

1. **SS vs. InGaAs Channel Thickness**
   - **SS** decreases as channel thickness increases.
   - **L_g = 20 nm**

2. **I_ON/I_OFF vs. InGaAs Channel Thickness**
   - **I_ON/I_OFF** increases as channel thickness increases.
   - **L_g = 20 nm**
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HEMT Simulator on nanoHUB.org

OMEN_FET:
- 2-D Schrödinger-Poisson solver
- Real-space effective mass quantum transport model
- Injection (white arrows) from Source, Drain, and Gate contacts
- HEMTs, Single- and Double-Gate devices
- Electron transport in Si and III-V
- Ballistic transport (no Scattering)
- Current Flow Visualization

http://nanoHUB.org/tools/omenhfet
Run your own simulations!
Conclusion and Outlook

- **Multiscale Modeling Approach**
  - EM transport including gate leakage
  - $m^*$ from tight-binding
- **Good Agreement with Experiments**
- **Scaling Considerations for 20nm Device**
- **HEMT Simulator Deployed on nanoHUB.org**
- **Challenges and Future Directions**
  - S/D contacts, high-k insulator, scattering, interface traps
Thank You!
Transfer Characteristics: $I_d-V_{gs}$ (2)

<table>
<thead>
<tr>
<th>$L_g$ [nm]</th>
<th>SS [mV/dec]</th>
<th>DIBL [mV/V]</th>
<th>$I_{ON}/I_{OFF}$</th>
<th>$V_{inj}$ [cm/s]</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 Expt.</td>
<td>107</td>
<td>169</td>
<td>$0.47\times10^3$</td>
<td></td>
</tr>
<tr>
<td>Sim.</td>
<td>105</td>
<td>145</td>
<td>$0.61\times10^3$</td>
<td>$3\times10^7$</td>
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<tr>
<td>40 Expt.</td>
<td>91</td>
<td>126</td>
<td>$1.38\times10^3$</td>
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<tr>
<td>Sim.</td>
<td>89</td>
<td>99</td>
<td>$1.86\times10^3$</td>
<td>$3.11\times10^7$</td>
</tr>
<tr>
<td>50 Expt.</td>
<td>85</td>
<td>97</td>
<td>$1.80\times10^3$</td>
<td></td>
</tr>
<tr>
<td>Sim.</td>
<td>89</td>
<td>91</td>
<td>$1.85\times10^3$</td>
<td>$3.18\times10^7$</td>
</tr>
</tbody>
</table>
Gate Leakage Mechanism

- Electrons tunnel from gate into InAs channel
- Tunneling barriers
  - InAlAs and InGaAs
  - Position dependent barriers
- Current crowding at edges (due to lower tunneling barriers)
- Barriers modulated by $\Phi_M$
Work Function Engineering (2)

Characteristics:

- **Same Gate Overdrive**
  - same thermionic current (source to drain)

- **Gate Fermi levels shifted by $\Delta \Phi_M$**
  - different tunneling barrier height

- **$\Phi_M = 4.7 \text{ eV}$**
  - tunnel through InAlAs only
  - larger $I_g$

- **$\Phi_M = 5.1 \text{ eV}$**
  - tunnel through InAlAs and InGaAs
  - lower $I_g$