10 nm CMOS: The Prospects for III-Vs

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Outline

• Introduction: Why III-Vs for CMOS?
• What have we learned from III-V HEMTs?
• What are the challenges for III-V CMOS?
• The prospects of 10 nm III-V CMOS
• Conclusions
Why III-Vs for CMOS?

- Si CMOS has entered era of “power-constrained scaling”:
  - CPU power density saturated at ~100 W/cm²
  - CPU clock speed saturated at ~4 GHz

Pop, Nano Res 2010

http://www.chem.utoronto.ca/~nlipkowi/pictures/clockspeeds.gif
Why III-Vs for CMOS?

• Under power-constrained scaling:

\[
\text{Power} = \text{active power} + \text{passive power}
\]

\[
\sim f CV_{\text{DD}}^2 N \quad \Rightarrow \quad N \uparrow \Rightarrow \quad V_{\text{DD}} \downarrow
\]

• But, \( V_{\text{DD}} \) scaling very weakly:
Why III-Vs for CMOS?

• Need scaling approach that allows $V_{DD}$ reduction

• Goal of scaling:
  – reduce footprint
  – extract maximum $I_{ON}$ for given $I_{OFF}$

• III-Vs:
  – Much higher injection velocity than Si
    $\rightarrow I_{ON} \uparrow$
  – Very tight carrier confinement possible
    $\rightarrow S \downarrow$
III-V CMOS: What are the challenges?

“To know where you are going, you first have to know where you are.”

We are starting from:

III-V High Electron Mobility Transistors
III-V HEMTs

- State-of-the-art: InAs-channel HEMT

- QW channel ($t_{ch} = 10$ nm):
  - InAs core ($t_{InAs} = 5$ nm)
  - InGaAs cladding
  - $\mu_{n,Hall} = 13,200 \text{ cm}^2/\text{V-sec}$
  - InAlAs barrier ($t_{ins} = 4$ nm)
  - Two-step recess
  - Pt/Ti/Mo/Au Schottky gate
  - $L_g = 30$ nm

Kim, IEDM 2008
III-V HEMTs

- $L_g=30$ nm InAs-channel HEMT

Kim, IEDM 2008

- Large current drive: $I_{on}=0.4$ mA/$\mu$m at $V_{DD}=0.5$ V
- Enhancement-mode FET: $V_T = 0.08$ V
- High transconductance: $g_{mpk} = 1.8$ mS/$\mu$m at $V_{DD}=0.5$ V
III-V HEMTs

- $L_g=30$ nm InAs-channel HEMT

- $S = 73$ mV/dec, DIBL = 85 mV/V, $I_{on}/I_{off}=\sim10^4$

- First transistor with both $f_T$ and $f_{max} > 600$ GHz

Kim, IEDM 2008
Scaling of III-V HEMTs: Benchmarking with Si

- Superior short-channel effects as compared to Si MOSFETs
- Lower gate delay than Si MOSFETs at lower $V_{DD}$
Scaling of III-V HEMTs: Benchmarking with Si

- $I_{ON} @ I_{OFF}=100 \text{ nA}/\mu\text{m}, V_{DD}=0.5 \text{ V}$: FOM that integrates short-channel effects and drive current

III-V HEMTs: higher $I_{ON}$ for same $I_{OFF}$ than Si
What can we learn from III-V HEMTs?

1. Very high electron injection velocity at the virtual source

\[ v_{\text{inj}} \equiv \text{electron injection velocity at virtual source} \]

- \( v_{\text{inj}} \) (InGaAs) increases with InAs fraction in channel
- \( v_{\text{inj}} \) (InGaAs) > 2\( v_{\text{inj}} \) (Si) at less than half \( V_{DD} \)
What can we learn from III-V HEMTs?

2. Quantum-well channel key to outstanding short-channel effects

- Dramatic improvement in electrostatic integrity in thin channel devices

Kim, IPRM 2010
What can we learn from III-V HEMTs?

3. Quantum capacitance less of a bottleneck than commonly believed

In$_{0.7}$Ga$_{0.3}$As channel
\[ t_{ch} = 13 \text{ nm} \]

InAs channel
\[ t_{ch} = 10 \text{ nm} \]

- Biaxial strain + non-parabolicity + strong quantization increase \( m_{\parallel}^* \rightarrow C_G \uparrow \)

Jin, IEDM 2009
Limit to III-V HEMT Scaling: Gate Leakage Current

InAs HEMT

- $L_g = 30$ nm
- $t_{ch} = 10$ nm
- $t_{ins} = 4$ nm
- $t_{ins} = 7$ nm
- $t_{ins} = 10$ nm

- $V_{DS} = 0.5$ V
- $I_{D}$
- $I_G$

$t_{ins} \downarrow \rightarrow I_G \uparrow$

$\rightarrow$ Further scaling requires high-K gate dielectric
The Challenges for III-V CMOS: III-V HEMT vs. Si CMOS

Critical issues:
- Schottky gate → MOS gate
- Footprint scaling [1000x too big!]
- Need self-aligned contacts
- Need p-channel device
- Need III-V on Si
The High-K/III-V System by ALD

- *Ex-situ* ALD produces high-quality interface on InGaAs:
  - Surface inversion demonstrated
  - $D_{it}$ in mid $\sim 10^{11}$ cm$^{-2}$.eV$^{-1}$ demonstrated

- $\text{Al}_2\text{O}_3/\text{In}_{0.52}\text{Ga}_{0.47}\text{As}$
- $\text{Al}_2\text{O}_3/\ln_{0.52}\text{Ga}_{0.47}\text{As}$

- $\text{Al}_2\text{O}_3/\text{In}_{0.65}\text{Ga}_{0.35}\text{As}$
- $\text{Al}_2\text{O}_3/\ln_{0.65}\text{Ga}_{0.35}\text{As}$

Lin, SISC 2008

Ye, 2010
In$_{0.7}$Ga$_{0.3}$As Quantum-Well MOSFET

- Direct MBE on Si substrate (1.5 µm buffer thickness)
- InGaAs buried-channel MOSFET (under 2 nm InP etch stop)
- 4 nm TaSiO$_x$ gate dielectric by ALD, TiN/Pt/Au gate
- $L_g = 75$ nm

Radosavljevic, IEDM 2009
**$\text{In}_{0.7}\text{Ga}_{0.3}\text{As Quantum-Well MOSFET}$**

2009 Intel InGaAs MOSFET
What can we expect from ~10 nm III-V NMOS at 0.5 V?

With thin InAs channel:

\[ I_D = q n_s v_{inj} \]
\[ = 1.6 \times 10^{-19} C \times 4 \times 10^{12} \text{ cm}^{-2} \times 3.8 \times 10^7 \text{ cm/s} \]
\[ = 2.4 \text{ mA/\mu m} \]

Assume \( R_S \) as in Si (~80 Ω.µm):

\[ I_D = 1.5 \text{ mA/\mu m} \]

Key requirements:

- High-K/III-V interface, thin channel do not degrade \( v_{inj} \)
- Obtaining \( R_S = 80 \text{ Ω.µm} \) at required footprint
- Acceptable short-channel effects

Three greatest worries!
Conclusions

• III-Vs attractive for CMOS: key for low $V_{DD}$ operation
  – Electron injection velocity in InAs > 2X that of Si at 1/2X $V_{DD}$
  – Quantum well channel yields outstanding short-channel effects
  – Quantum capacitance less of a limitation than previously believed

• Impressive recent progress on III-V CMOS
  – Ex-situ ALD and MOCVD on InGaAs yield interfaces with unpinned Fermi level and low defect density
  – Sub-100 nm InGaAs MOSFETs with $I_{ON} >$ than Si at 0.5 V demonstrated

• Lots of work ahead:
  – Demonstrate 10 nm III-V MOSFET that is better than Si
  – P-channel MOSFET
  – Manufacturability, reliability