Impact of Gate Placement on RF Degradation in GaN HEMTs

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Motivation

• RF reliability – main concern in GaN HEMT RF power amplifier
• Compared to DC stress, little known about degradation mechanisms under RF stress
  – $P_{\text{out}} \downarrow$, Gain $\downarrow$
  – $I_D \downarrow$, dispersion $\uparrow$, $g_m \downarrow$, $|I_G| \uparrow$
  – RF introduces more degradation than DC
    [Conway, IRPS 2007; Joh, ROCS 2008; Chini, IEDM 2009; Joh, IEDM 2010]

• Goal:
  – Develop methodology for RF reliability studies
  – Identify dominant RF degradation mechanisms
  – Correlate RF and DC reliability
Experimental Setup

Accel-RF AARTS RF10000-4/S system:
- two 2-4 GHz channels
- two 7-12 GHz channels
- Max $P_{in} = 30$ dBm
- $T_{base} = 50-200 \, ^\circ C$

Accel-RF system augmented with:
- external instrumentation for DC/pulsed characterization
- software to control external instrumentation and extract DC and RF FOMs
RF Experiment Flowchart: Conventional Approach

Limitations:
- Bias point shifts during stress
- Limited RF characterization
- No DC characterization
- No trap characterization
- If examining different RF conditions, RF characterization confusing

START

RF Stress

T_{stress}

P_{out}, PAE, Gain, I_{DQ}, I_{GQ}

END
RF Experiment Flowchart: Improved Approach

- **Short characterization:**
  - Every few minutes at $T_{\text{base}}=50 \, ^\circ\text{C}$
  - DC FOMs: $I_{\text{Dmax}}, R_S, R_D, V_T, I_{\text{Goff}}, \ldots$
  - RF FOMs @ $V_{\text{DS}}=28 \, \text{V} \& I_{\text{DQ}}=100 \, \text{mA/mm}$
    - Saturated conditions ($P_{\text{in}}=23 \, \text{dBm}$): $P_{\text{out,sat}}, G_{\text{sat}}, \text{PAE}$
    - Linear conditions ($P_{\text{in}}=10 \, \text{dBm}$): $G_{\text{lin}}$

- **Full Characterization:**
  - After key events at room temperature
  - Full DC I-V sweep
  - Current collapse (after 1" $V_{\text{DS}}=0, V_{\text{GS}}=-10 \, \text{V}$ pulse)
  - Full RF power sweep @ $V_{\text{DS}}=28 \, \text{V}$, $I_{\text{DQ}}=100 \, \text{mA/mm}$

- **Detrapping:** $T_{\text{base}}=100 \, ^\circ\text{C}$ for 30 mins
**$P_{\text{in}}$ Step-Stress: Centered Gate**

- **Motivation:**
  - higher $P_{\text{in}}$ $\rightarrow$ larger V waveform at output

- **MMIC:**
  - single-stage internally-matched
  - 4x100 μm GaN HEMT
  - Gate placed at the center btw S & D

- **Step $P_{\text{in}}$ stress:**
  - $V_{DS} = 40$ V, $I_{DQ} = 100$ mA/mm
  - $P_{\text{in}} = 0$ (DC), 1, 20-27 dBm
  - 300 min stress at each step
  - $T_{\text{stress}} = 50$ °C
Characterization during RF Stress

- RF FOMs changing because $P_{\text{in}}$ changing
- Degradation apparent but not easily quantifiable
DC FOM during Short Characterization

- Little degradation under DC and low $P_{in}$
- Beyond $P_{in}=20$ dBm:
  - RF induces degradation of $I_{Dmax}$ and $R_D$
  - Sharp degradation in $I_{Goff}$
• Similar critical behavior. Beyond $P_{\text{in}}=20$ dBm:
  — Sharp $P_{\text{out}}$ degradation
  — permanent degradation of $I_{\text{Dmax}}$
  — Evidence of new traps created (increased CC)
Structural Degradation (Planar View)

- Pit formation along the drain side of gate edge
- Same degradation mechanism as in DC high field OFF-state
Correlation between DC and RF FOM

- **Good correlation** between $P_{\text{out}}$ and $I_{\text{Dmax}}$ degradation
  
  $\Delta P_{\text{out}} = 1 \text{ dB} \iff \Delta I_{\text{Dmax}} = 9\%$

Short characterization @ 50 °C
Step $P_{in}$ Stress: Offset Gate

- More degradation under RF stress @ high $P_{in}$
- No $I_{Goff}$ degradation ($\text{high } V_{crit}$)
- Degradation in $I_{Dmax}$ and $R_S$, not in $R_D$
- No structural degradation

Joh, IEDM 2010
Pulsed Stress: High-power State

- High-power stress not accessible in DC $\rightarrow$ pulsed stress
- Pulsed stress reproduces large $R_S$ degradation in offset gate
- No $R_S$ degradation in centered gate

100 pulses, 500 us, 0.05% duty
$I_{Dpulse} = 950$ mA/mm
Summary

• Developed new RF reliability testing methodology

• Critical behavior in RF stress on centered gate:
  – $P_{\text{in}} \uparrow \rightarrow P_{\text{out}} \downarrow$ (>> DC stress)
  – $I_{\text{Dmax}} \downarrow$, current collapse $\uparrow$, $I_{\text{Goff}} \uparrow$
  – Good correlation between DC and RF FOMs
  – Structural degradation on drain-side gate edge
  – Same degradation mechanism under high-voltage OFF-state DC stress

• Offset gate:
  – Different degradation mechanism is present
  – Significant $R_S$ degradation