III-V CMOS: What have we learned from HEMTs?

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Outline

• Why III-Vs for CMOS?

• What have we learned from III-V HEMTs

• III-V CMOS device design and challenges

• Conclusions
CMOS scaling in the 21st century

- Si CMOS has entered era of “power-constrained scaling”:
  - Microprocessor power density saturated at ~100 W/cm²
  - Microprocessor clock speed saturated at ~ 4 GHz

Pop, Nano Res 2010
Consequences of Power Constrained Scaling

Power = active power + stand-by power

$P_A \sim f C V_{DD}^2 N \Rightarrow N \uparrow \Rightarrow V_{DD} \downarrow$

- Transistor scaling requires reduction in supply voltage
- Not possible with Si: performance degrades too much
How III-Vs allow further $V_{DD}$ reduction?

- Goals of scaling:
  - reduce transistor footprint
  - extract maximum $I_{ON}$ for given $I_{OFF}$
How III-Vs allow further $V_{DD}$ reduction?

- **Goals of scaling:**
  - reduce transistor footprint
  - extract maximum $I_{ON}$ for given $I_{OFF}$

- **III-Vs:**
  - higher electron velocity than Si $\rightarrow I_{ON} \uparrow$
  - tight carrier confinement in quantum well $\rightarrow S \downarrow \rightarrow V_{DD} \downarrow$
What have we learned from III-V HEMTs?

State-of-the-art: InAs HEMTs

- QW channel ($t_{ch} = 10$ nm):
  - InAs core ($t_{InAs} = 5$ nm)
  - InGaAs cladding
- $\mu_{n,\text{Hall}} = 13,200$ cm$^2$/V-sec
- InAlAs barrier ($t_{ins} = 4$ nm)
- Ti/Pt/Au Schottky gate
- $L_g=30$ nm

Kim, EDL 2010
\( L_g = 30 \text{ nm InAs HEMT} \)

- Large current drive: \( I_{\text{ON}} > 0.5 \text{ mA/\( \mu \text{m} \)) at \( V_{\text{DD}} = 0.5 \text{ V} \)
- \( V_T = -0.15 \text{ V}, R_S = 190 \text{ ohm.\( \mu \text{m} \))
- High transconductance: \( g_{mpk} = 1.9 \text{ mS/\( \mu \text{m} \)) at \( V_{\text{DD}} = 0.5 \text{ V} \)
**L_g=30 nm InAs HEMT**

Kim, EDL 2010

- Only transistor of any kind with both $f_T$ and $f_{\text{max}} > 640$ GHz
- $S = 74$ mV/dec, DIBL = 80 mV/V, $I_{\text{on}}/I_{\text{off}} \sim 5\times10^3$
- All FOMs at $V_{\text{DD}}=0.5$ V
InAs HEMTs: Benchmarking with Si

- FOM that integrates short-channel effects and transport:
  \( I_{\text{ON}} @ I_{\text{OFF}} = 100 \, \text{nA/\mu m}, \quad V_{DD} = 0.5 \, \text{V} \)

InAs HEMTs: higher \( I_{\text{ON}} \) for same \( I_{\text{OFF}} \) than Si: Why?
Why high $I_{ON}$?

1. Very high electron injection velocity at the virtual source

- $v_{inj}(\text{InGaAs})$ increases with InAs fraction in channel
- $v_{inj}(\text{InGaAs}) > 2v_{inj}(\text{Si})$ at less than half $V_{DD}$
- ~100% ballistic transport at $L_g \sim 30$ nm

Kim, IEDM 2009
Liu, Springer 2010
Why high $I_{ON}$?

2. Quantum capacitance less of a bottleneck than previously believed

Biaxial strain + non-parabolicity + strong quantization:

$m_{||}^* \uparrow \rightarrow C_G \uparrow \rightarrow n_s \uparrow \rightarrow I_{ON} \uparrow$
Why high $I_{ON}$?

3. Sharp subthreshold swing due to quantum-well channel

- Dramatic improvement in short-channel effects with thin channel
- Thin channel does not degrade $v_{inj}$ at $L_g \sim 40$ nm (Kim, IPRM 2011)
Limit to III-V HEMT Scaling: Gate Leakage Current

InAs HEMT
L_g = 30 nm
t_{ch} = 10 nm

V_{DS} = 0.5 V

\[ I_{D}, I_{G} \text{ [A/\mu m]} \]

\[ I_{D} \quad I_{G} \]

\[ V_{GS} \text{ [V]} \]

\[ t_{ins} = 10 \text{ nm} \]
\[ t_{ins} = 7 \text{ nm} \]
\[ t_{ins} = 4 \text{ nm} \]

\[ t_{ins} \downarrow \rightarrow I_{G} \uparrow \]
\[ \rightarrow \text{Further scaling requires high-K gate dielectric} \]
III-V CMOS: device design and challenges

Modern III-V HEMT vs. modern Si MOSFET:

- What do we preserve?
- What do we change?
III-V CMOS: HEMT features worth preserving

- Quantum-well channel: key to scalability
- Undoped channel:
- InAs-rich channel: for high mobility and velocity
- Buried-channel design:
- Raised source and drain regions: essential for scalability
- Undoped QW channel in extrinsic regions: key to low access resistance
III-V CMOS: HEMT features to change

- **Schottky gate**: need MOS gate with very thin high-K dielectric
- **T-gate**: need rectangular gate
- **Barrier under contacts**: need to eliminate
- **Alloyed ohmic contacts**: change to refractory ohmic contacts
- **Source and drain contacts**: need self-aligned with gate
- **Footprint**: need to reduce by 1000 X!

HEMT

QW-MOSFET
III-V CMOS: other critical needs

- p-channel MOSFET: with performance >1/3 that of n-MOSFET
- Co-integration of n-FET and p-FET on Si: compact, planar surface
III-V CMOS: other designs

Etched S/D QW-MOSFET

Regrown S/D QW-MOSFET

FinFET

Gate-all-around nanowire FET
The high-water mark: Intel’s InGaAs Quantum-Well MOSFET

- Direct MBE on Si substrate (1.5 μm buffer thickness)
- InGaAs buried-channel MOSFET (under 2 nm InP barrier)
- 4 nm TaSiO\textsubscript{x} gate dielectric by ALD, L\textsubscript{g}=75 nm
- First III-V QW-MOSFET with better performance than Si

Radosavljevic, IEDM 2009
More recent notable work

**InAs Nanoribbon MOSFETs on Insulator (UC Berkeley)**
Ko, Nature 2010

**Al$_2$O$_3$/InGaSb QW-MOSFET (Stanford)**
Nainani, IEDM 2010

**InGaAs FinFET (Purdue, Intel)**
Wu, IEDM 2009
Radosavljevic, IEDM 2010

**Aspect Ratio Trapping (Amberwave)**
Fiorenza, ECS 2010

**Self-aligned QW-FET (MIT)**
Kim, IEDM 2010

**Ge p-type QW-MOSFET (Intel)**
Pillarisetty, IEDM 2010
Conclusions

- **III-V HEMTs suggest strong potential for III-V CMOS:**
  - InAs electron injection velocity > 2x that of Si at 1/2x $V_{DD}$
  - Quantum capacitance less of a bottleneck than previously believed
  - Quantum-well channel yields outstanding short-channel effects

- **Impressive recent progress on III-V CMOS**
  - Sub-100 nm InGaAs MOSFETs with $I_{ON}$ > than Si at 0.5 V demonstrated

- **Lots of work ahead**
  - Demonstrate ~10 nm III-V N-MOSFET that is better than Si
  - P-channel MOSFET
  - N-channel + P-channel cointegration on Si