High-Voltage DC and RF Power Reliability of GaN HEMTs

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Breakthrough RF-mmw power in GaN HEMTs

$P_{\text{out}} > 40 \text{ W/mm}, \text{ over } 10X \text{ GaAs!}$

Wu, DRC 2006

Micovic, MTT-S 2010

Micovic, Cornell Conf 2010

94-95 GHz MMIC PAs:
GaN HEMTs in the field

Counter-IED Systems (CREW)

200 W GaN HEMT for cellular base station
Kawano, APMC 2005

100 mm GaN-on-SiC volume manufacturing
Palmour, MTT-S 2010
Recent great strides in RF power reliability

28 V RF oper. life > 2 years (X-band, 3 dB comp., ~150°C)

Kolias, MTT-S 2010

MTTF=1x10^7 h at 47 V (C-band, 5 dB comp., ~150°C)
Yamasaki, MTT-S 2010

MTTF=7x10^7 h at 28 V (40 GHz, 1.5 dB comp., ~150°C)
Heying, MTT-S 2010
Dominant degradation mechanisms under RF stress?

• In general:
  – RF stress $\rightarrow P_{\text{out}} \downarrow$, Gain $\downarrow$, $I_{D_{\text{max}}} \downarrow$, $|I_G| \uparrow$, $V_T$ shift, dispersion $\uparrow$
  – RF introduces more degradation than DC
  – RF stress accelerated by $V_{DQ}$, $P_{in}$, $T_j$


• Indications of two competing mechanisms:
  – Trap creation and trapping?
  – Field-driven structural degradation?

Chini, EUMW 2009

Rozman, ROCS 2009; Chini, IEDM 2009

Dammann, IRPS 2010
Outline

1. RF power reliability concerns
2. Methodology for RF reliability experiments
3. Electrical and structural results
4. Discussion: the role of gate placement
5. Conclusions
RF power reliability concerns

ON DC stress:
- Mostly benign

High-power DC stress:
- Not accessible to DC stress experiments
- Device blows up instantly

OFF and semi-ON high-voltage DC stress:
- Degradation of \( I_{D_{\text{max}}} \), \( R_D \), \( I_{G_{\text{off}}} \)
- \( V_T \) shift
- Electron trapping
- Trap creation
- Formation of grooves and pits under drain-end of gate

Graph showing RF load line and DC stress regions.
RF experiment flowchart: conventional approach

Limitations:
- Bias point shifts during stress
- Limited RF characterization
- No DC characterization
- No trap characterization
- If examining different RF conditions, RF characterization confusing
RF experiment flowchart: improved approach (I)

New features:
• RF and DC characterization under standardized conditions
• At beginning, end and periodically through experiment

Limitations:
• Limited characterization
• Characterization temperature cannot be too different from stress temperature
• Cannot separate trapping from “permanent” degradation
RF experiment flowchart: improved approach (II)

New features:
- Comprehensive DC, RF and pulsed characterization under standardized conditions (RT)
- At beginning, end, and during experiment
- Detrapping step to enable trap characterization

Flowchart:
- **START**
  - **Detrapping**
  - **Full Characterization (DC, RF, CC)**
  - **T_{base}**
  - **Short Characterization (DC, RF)**
  - **T_{stress}**
  - **RF Stress**
  - **Key Event?**
    - **YES**
      - **END: detrapping + Full characterization**
    - **NO**

Setup for RF reliability studies

Accel-RF AARTS RF10000-4/S system:
• two 2-4 GHz channels
• two 7-12 GHz channels
• Max $P_{\text{in}}$ = 30 dBm
• $T_{\text{base}}$ = 50-200 °C

Augmented with:
• external instrumentation for DC/pulsed characterization
• software to control external instrumentation and extract DC and RF FOMs
RF-stress experiments

START

Detrapping

Full Characterization (DC, RF, CC)

RT

Short Characterization (DC, RF)

T_{base}=50°C

RF (DC) Stress

T_{stress}

YES

NO

Key Event?

YES

END: detrapping + Full characterization

NO

T_{base}=100°C for 30 mins

- Full DC I-V sweeps
- RF power sweep @ V_{DS}=28 V, I_{DQ}=100 mA/mm
- Current collapse (after 1” V_{DS}=0, V_{GS}=-10 V pulse)
- Room temperature

- DC FOMs: I_{D_{max}}, R_{S}, R_{D}, V_{T}, I_{Goff}, ...
- RF FOMs @ V_{DS}=28 V, I_{DQ}=100 mA/mm
  - Saturated conditions (P_{in}=23 dBm): P_{out,sat}, G_{sat}, PAE
  - Linear conditions (P_{in}=10 dBm): G_{lin}
- Every few minutes at T_{base}=50°C
RF stress experiments: $P_{\text{in}}$ step-stress

- **Motivation:**
  - higher $P_{\text{in}} \rightarrow$ larger $V$ waveform at output

- **MMIC:**
  - single-stage internally-matched
  - 4x100 $\mu$m GaN HEMT (OFF-state $V_{\text{crit}} > 60$ V at RT)
  - Gate centered in S-D gap

- **Step $P_{\text{in}}$ stress:**
  - $V_{DS} = 40$ V, $I_{DQ} = 100$ mA/mm
  - $P_{\text{in}} = 0$ (DC), 1, 20-27 dBm
  - 300 min stress at each step
  - $T_{\text{stress}} = 50$ °C ($T_j = 110-230$ °C)
Evolution of RF stress

- $P_{in}$ changing $\rightarrow$ RF FOMs changing
- Degradation apparent but not easily quantifiable
RF FOM during short characterization

- Mild degradation under DC and low $P_{in}$
- Adding RF increases degradation: $P_{in} \uparrow \Rightarrow P_{out} \downarrow$
DC FOM during short characterization

- Mild degradation under DC and low $P_{in}$
- At $P_{in} = 20$ dBm, step degradation in $I_{Goff}$
- Beyond $P_{in} = 20$ dBm, increasing degradation of $I_{Dmax}$ and $R_D$
DC/RF/CC full characterization

Beyond $P_{in}=20$ dBm:
- Sharp $P_{out}$ degradation
- Permanent degradation of $I_{D_{max}}$
- Increased CC $\rightarrow$ evidence of new trap creation
Structural degradation (planar view)

SEM

AFM

• Pit formation along drain end of gate edge
• Similar to DC high voltage OFF-state stress

DC OFF-state stress, $V_{DG}=50$ V,
1000 min, $\sim150^\circ$C
Makaram, APL 2010
HV OFF-state DC vs. RF power degradation

Similar pattern of degradation:

<table>
<thead>
<tr>
<th></th>
<th>HV OFF-state DC</th>
<th>RF power</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{D_{\text{max}}}$</td>
<td>$\downarrow$ beyond $V_{\text{crit}}$</td>
<td>$\downarrow$ beyond $P_{\text{in-crit}}$</td>
</tr>
<tr>
<td>$R_D$</td>
<td>$\uparrow$ beyond $V_{\text{crit}}$</td>
<td>$\uparrow$ beyond $P_{\text{in-crit}}$</td>
</tr>
<tr>
<td>$R_S$</td>
<td>small increase</td>
<td>small increase</td>
</tr>
<tr>
<td>$I_{\text{Goff}}$</td>
<td>$\uparrow$ beyond $V_{\text{crit}}$</td>
<td>$\uparrow$ beyond $P_{\text{in-crit}}$</td>
</tr>
<tr>
<td>Current Collapse</td>
<td>$\uparrow$ beyond $V_{\text{crit}}$</td>
<td>$\uparrow$ beyond $P_{\text{in-crit}}$</td>
</tr>
<tr>
<td>Permanent $I_{D_{\text{max}}}$</td>
<td>$\downarrow$ beyond $V_{\text{crit}}$</td>
<td>$\downarrow$ beyond $P_{\text{in-crit}}$</td>
</tr>
<tr>
<td>Pits under drain end of gate</td>
<td>Yes</td>
<td>Yes</td>
</tr>
<tr>
<td>Pits under source end of gate</td>
<td>No</td>
<td>No</td>
</tr>
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</table>

High $V$ end of load line responsible for degradation
Step $P_{in}$ stress: **Offset Gate**

Offset gate devices ($L_{GS}<L_{GD}$): OFF-state $V_{crit} > 80$ V at $T=150^\circ$C

- **Increased degradation under high $P_{in}$**
- **No $I_{Goff}$ degradation**
- **Degradation of $I_{Dmax}$ and $R_S$, not $R_D$**

Joh, IEDM 2010
HV OFF-state DC vs. RF power degradation

Different pattern of degradation:

<table>
<thead>
<tr>
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<th>HV OFF-state DC</th>
<th>RF power</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{D\text{max}}$</td>
<td>↓ beyond $V_{\text{crit}}$</td>
<td>↓ beyond $P_{\text{in-crit}}$</td>
</tr>
<tr>
<td>$R_D$</td>
<td>↑ beyond $V_{\text{crit}}$</td>
<td>↑ beyond $P_{\text{in-crit}}$</td>
</tr>
<tr>
<td>$R_S$</td>
<td>small increase</td>
<td>↑↑ beyond $P_{\text{in-crit}}$</td>
</tr>
<tr>
<td>$I_{G\text{off}}$</td>
<td>↑ beyond $V_{\text{crit}}$</td>
<td>No</td>
</tr>
<tr>
<td>Current Collapse</td>
<td>↑ beyond $V_{\text{crit}}$</td>
<td>↑ beyond $P_{\text{in-crit}}$</td>
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High V end of load line NOT responsible for degradation
High-power pulsed stress

• High-power stress not accessible in DC → pulsed stress
• Offset-gate and centered-gate devices on same wafer:

- Pulsed stress reproduces $R_S$ degradation in offset gate device
- No $R_S$ degradation in centered gate

100 pulses, 500 μs, 0.05% duty
$I_{D\text{pulse}}=950$ mA/mm

High power region of load line responsible for degradation
Summary

• New RF reliability testing methodology developed
• Under RF stress, degradation worse than at DC bias point
• Different patterns of RF degradation observed:
  – In some device designs, it reproduces HV OFF-state DC degradation (field driven)
  – In other device designs, degradation pattern correlates with high-power pulsed stress (power driven?)

→ DC reliability not good predictor for RF reliability
→ Need for fundamental studies of RF reliability