InAs HEMTs: the path to THz electronics?

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Short Course on: High-Performance narrow-bandgap HEMT technology for advanced microwave front-ends: Towards the end of the roadmap?

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III-V HEMT: record $f_T$ vs. time

Current record: $f_T = 660$ GHz
Leuther IPRM 2011 (Fraunhofer Inst.)

For >20 years, record $f_T$ obtained on InGaAs-channel HEMTs
III-V HEMT: record $f_T$ vs. time

Well balanced devices: $f_T=644$ GHz, $f_{\text{max}}=680$ GHz at same bias point
Kim EDL 2010 (MIT)

InGaAs-channel HEMTs offer record balanced $f_T$ and $f_{\text{max}}$
Record $f_T$ III-V HEMTs: megatrends

Over time: $L_g \downarrow$, $\lnxGa_{1-x}$As channel $x_{\ln As} \uparrow$
Record $f_T$ III-V HEMTs: megatrends

Over time: $t_{ch} \downarrow$, $t_{ins} \downarrow$
Outline

1. Example of high-frequency InAs HEMT
2. $f_T$ measurements
3. $f_T$ analysis
4. How to improve $f_T$
5. Limits to HEMT scaling and future prospects
1. Example of high-frequency InAs HEMT

$L_g=30$ nm InAs HEMT

- QW channel ($t_{ch}=10$ nm):
  - InAs core ($t_{InAs}=5$ nm)
  - InGaAs cladding
  - $\mu_{n,Hall}=13,200$ cm$^2$/V-sec
- InAlAs barrier ($t_{ins}=4$ nm)
- Ti/Pt/Au Schottky gate
- $L_g=30$ nm
- $L_{side}=150$ nm

Kim, EDL 2010
\( L_g = 30 \text{ nm InAs HEMT} \)

- Large current drive: \( I_{ON} > 0.5 \text{ mA/\mu m} \) at \( V_{DD} = 0.5 \text{ V} \)
- \( V_T = -0.15 \text{ V} \), \( R_S = 190 \text{ Ohm.\mu m} \)
- High transconductance: \( g_{mpk} = 1.9 \text{ mS/\mu m} \) at \( V_{DD} = 0.5 \text{ V} \)

Kim, EDL 2010
**L_g=30 nm InAs HEMT**

- Only transistor of any kind with both $f_T$ and $f_{\text{max}} > 640$ GHz at same bias point
- Subthreshold characteristics:
  - $S = 74 \text{ mV/dec}$, DIBL = 80 mV/V, $I_{\text{on}}/I_{\text{off}} \sim 5 \times 10^3$
2. $f_T$ measurements

- Extraordinary claims demand extraordinary evidence!

- Verification of $f_T$ and $f_{\text{max}}$ measurements:
  1. Gummel technique
  2. Small-signal equivalent circuit model
  3. Measurements on multiple devices
  4. Measurements on multiple test benches
Gummel technique for $f_T$ extraction

In one-pole system:

$$h_{21}(f) = \frac{h_{21}(DC)}{1 + jf \frac{h_{21}(DC)}{f_T}}$$

Then:

$$\text{Im} \left[ \frac{1}{h_{21}(f)} \right] = \frac{f}{f_T}$$

Slope gives $f_T$

Kim, EDL 2008

Gummel, Proc IEEE 1969
**$f_T$ extraction from equivalent-circuit model**

Small-signal equivalent circuit model in linear and saturation regimes at $V_{GS}$ of peak $f_T$:

Extrapolation from small-signal model yields:

→ $f_T = 648$ GHz
→ $f_{max} = 686$ GHz

Also model S parameters (see below)
Measurements on multiple devices and systems

Measurements of one device in three different test benches:

<table>
<thead>
<tr>
<th></th>
<th>8510C @MIT</th>
<th>8510C @TSC</th>
<th>PNA @UCSB</th>
<th>Avg.</th>
<th>STD</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_T ) [GHz]</td>
<td>From ( H_{21} )</td>
<td>645</td>
<td>645</td>
<td>643</td>
<td>644.3</td>
</tr>
<tr>
<td></td>
<td>From Gummel’s approach</td>
<td>644</td>
<td>644</td>
<td>645</td>
<td>644.3</td>
</tr>
<tr>
<td>( f_{\text{max}} ) [GHz]</td>
<td></td>
<td>681</td>
<td>686</td>
<td>677</td>
<td>681.3</td>
</tr>
</tbody>
</table>

Kim, EDL 2010

Measurement of three devices on one test bench:

\[ f_T = 645, 644, 644 \text{ GHz}. \]

All measurements at same bias point: \( V_{GS} = 0.2 \text{ V}, V_{DS} = 0.5 \text{ V} \)
3. $f_T$ analysis

- First-order $f_T$ expression for HEMT:

$$f_T = \frac{1}{2\pi} \frac{g_{mi}}{C_{gs} + C_{gd} + g_{mi}(R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]}$$
Break out parasitic capacitances

- Capacitance components:

\[ C_{gs} = C_{gsi} + C_{gsext} \quad C_{gd} = C_{gdi} + C_{gdext} \]
Delay time analysis

• Delay time:

\[ \tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par} \]

• Components of delay time:

\[ \tau_t = \frac{C_{gsi} + C_{gdi}}{g_{mi}} = \frac{L_g}{v_e} \]

Extrinsic delay

\[ \tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}} \]

Intrinsic delay (transit time)

\[ \tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd}) \frac{g_{oi}}{g_{mi}}] \]

Parasitic delay
Extraction of parasitic capacitances

- Need devices with different $L_g$
- Bias them at same $V_{GS}$ overdrive around peak $f_T$ point
- Extract small-signal equivalent circuit models
- Study $L_g$ scaling behavior of $C_{gs}$ and $C_{gd}$

InAs HEMTs
($f_t=601$ GHz, $f_{max}=609$ GHz at $L_g=30$ nm)
Kim, IEDM 2008
Delay components of $L_g=30$ nm InAs HEMT

Delay time from $f_t$: $\sim 265$ fs
  - Intrinsic delay: $\sim 59$ fs
  - Extrinsic delay: $\sim 117$ fs
  - Parasitic delay: $\sim 80$ fs
  - Unaccounted: $\sim 9$ fs

Least significant, yields $v_e=5.1 \times 10^7$ cm/s

Most significant

InAs HEMTs
($f_t=601$ GHz, $f_{\text{max}}=609$ GHz at $L_g=30$ nm)
Kim, IEDM 2008
Scaling of delay components

InAs HEMTs
(f_t=601 GHz, f_max=609 GHz at L_g=30 nm)
Kim, IEDM 2008

\(\tau_{\text{ext}}\) and \(\tau_{\text{par}}\) do not scale, become dominant for \(L_g < 60\) nm
4. How to improve $f_T$

- **Intrinsic delay:**

  \[
  \tau_t = \frac{C_{gsi} + C_{gdi}}{g_{mi}} = \frac{L_g}{v_e}
  \]

  $\rightarrow L_g \downarrow$ (without degrading $g_{mi}$)

  $\rightarrow v_e \uparrow \rightarrow$ channel engineering

- **Extrinsic delay:**

  \[
  \tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}
  \]

  $\rightarrow C_{gsext}, C_{gdext} \downarrow \rightarrow$ gate engineering

  $\rightarrow g_{mi} \uparrow \rightarrow$ harmonious scaling
How to improve $f_T$

- Parasitic delay:

\[ \tau_{par} = (R_S + R_D) \left[ C_{gd} + (C_{gs} + C_{gd}) \frac{g_{oi}}{g_{mi}} \right] \]

$\rightarrow R_S + R_D \downarrow$
$\rightarrow$ increase electrostatic integrity: $g_{oi}/g_{mi} \downarrow$
How far can we expect to go?

$f_t = 1$ THz feasible even at $L_g = 30$ nm

$V_{DS} = 0.5$ V

Modeled iedm 08

+ 50% Reduction in $R_s$ and $R_d$

+ 50% Reduction in $C_{gext}$
a) $R_S + R_D \downarrow$

- In typical HEMTs:
  - large G-S, G-D gaps
  - barrier in extrinsic region
  - limited electron concentration in extrinsic channel

Kim, IEDM 2010
Approaches to reducing barrier and $n_{s,\text{ext}} \uparrow$

- InAs-rich InAlAs sub-barrier:

$L_g = 40 \text{ nm} \ \text{In}_{0.7}\text{Ga}_{0.3}\text{As HEMT:}$

$R_s \sim 170 \text{ Ohm.}\mu\text{m}$

$f_T = 530 \text{ GHz at } V_{DS} = 0.7 \text{ V}$

Kim, Electron Lett 2011
Approaches to reducing barrier and $n_{s,ext}$ ↑

- Dual delta-doping in barrier:

Kim, IEDM 2010
Approaches to reducing $L_{GS}$ and $L_{GD}$

Self-aligned process:

- Heterostructure with dual delta doping in InAlAs
- Dry-etched Mo contacts: $R_c = 7 \text{ Ohm} \cdot \text{um}$, stable to 600 °C
- $L_G=50 \text{ nm}$, $R_S=144 \text{ Ohm} \cdot \text{um}$, $g_m=2.2 \text{ mS/um}$ @ $V_{DS}=0.5 \text{ V}$
$L_g=60$ nm self-aligned $\text{In}_{0.7}\text{Ga}_{0.3}$As HEMT

- Good agreement between modeled and measured HF characteristics
- Highest $f_T$ and $f_{\text{max}}$ at $L_g \geq 60$ nm of any FET

$V_{\text{GS}} = 0.2$ V, $V_{\text{DS}} = 0.6$ V
$W_g = 2 \times 20$ $\mu$m
$L_g = 60$ nm

$S_{21}/10$
$S_{12}$
$S_{22}$
$S_{11}$

freq (500.0MHz to 700.0GHz)

Kim, IEDM 2010
b) Increase electrostatic integrity: $g_{oi}/g_{mi} \downarrow$

Sources of output conductance in InAs HEMTs:
- impact ionization: slow $\rightarrow$ irrelevant at RF
- drain-induced barrier lowering (DIBL)

Kim, IPRM 2009
Drain-Induced Barrier Lowering (DIBL)

- Negative shift of $V_T$ with $V_{DS}$
- Due to reduction in channel barrier as $V_{DS} \uparrow$

DIBL Figure of Merit:

$$DIBL = \left. \frac{dV_T}{dV_{DS}} \right|_{V_{GS}}$$

30 nm InAs HEMT

Kim, EDL 2010

DIBL = 80 mV/V
Drain-Induced Barrier Lowering (DIBL)

Factors affecting DIBL:
- Gate length: $L_g$
- Channel thickness: $t_{ch}$
- Barrier thickness: $t_{ins}$
- Side etch length: $L_{side}$

Kim, ISDRS 2007
Kim, TED 2008
Kim, IPRM 2010
The role of $L_{\text{side}}$ in $f_T$

As $L_{\text{side}}$ ↑

$\rightarrow g_{oi} \downarrow \rightarrow \tau_{\text{par}} \downarrow$

$\rightarrow C_{g\text{ext}}, C_{g\text{d ext}} \downarrow \rightarrow \tau_{\text{ext}} \downarrow$

$\rightarrow R_S, R_D \uparrow \rightarrow \tau_{\text{par}} \uparrow$

Kim, JSTS 2006

Suemitsu, TED 2002

There is an optimum $L_{\text{side}}$ which depends on rest of device design.
The role of $t_{\text{ins}}$ in $f_T$

As $t_{\text{ins}}$ ↓
→ $g_{oi}$ ↓ → $\tau_{\text{par}}$ ↓
→ $g_{mi}$ ↑ → $\tau_{\text{par}}$ ↓, $\tau_{\text{ext}}$ ↓
→ $R_S, R_D$ ↑ → $\tau_{\text{par}}$ ↑

$f_T$ tends to improve as $t_{\text{ins}}$ ↓

Kim, TED 2008

Kim, IEDM 2008
The role of $t_{ch}$ in $f_T$

As $t_{ch} \downarrow$
- $g_{oi} \downarrow \rightarrow \tau_{par} \downarrow$
- $g_{mi} \uparrow \rightarrow \tau_{par} \downarrow$, $\tau_{ext} \downarrow$
- $R_s, R_D \uparrow \rightarrow \tau_{par} \uparrow$

$f_T$ tends to improve as $t_{ch} \downarrow$

Kim, IPRM 2009

In$_{0.7}$Ga$_{0.3}$As PHEMTs

$f_T$, $f_{max}$

$L_g$ [nm]

$V_{DS} = 0.5$ V
c) $L_g \downarrow$ without degrading $g_{mi}$

Harmonious scaling required: as $L_g \downarrow \rightarrow t_{ch} \downarrow$, $t_{ins} \downarrow$
Aspect ratio of record $f_t$ devices

Channel aspect ratio: $L_g/t_{ch}$

Insulator aspect ratio: $L_g/t_{ins}$

- Channel aspect ratio between 2 and 4
- Insulator aspect ratio between 2 and 8 (2 likely an underestimate)

Our work: dimensions verified by XTEM
5. Limits to HEMT scaling and future prospects

Barrier thickness scaling limited by $I_G$

![Graph showing InAs HEMT characteristics with $L_g = 30$ nm, $t_{ch} = 10$ nm, $L_{side} = 150$ nm, $t_{ins} = 4$ nm, $t_{ins} = 7$ nm, and $t_{ins} = 10$ nm, for $V_{DS} = 0.5$ V. Diagram by del Alamo, IPRM 2011.]
Alternative insulators

High-K dielectrics being pursued for III-V CMOS

→ huge opportunity for THz HEMT electronics!

Radosavljevic, IEDM 2009
Limits to HEMT scaling

Deep channel thickness scaling degrades performance:

$\Rightarrow R_S \uparrow \Rightarrow f_T \downarrow$

InAs HEMT, $L_{side} = 80$ nm, $t_{ins} = 5$ nm

Noticeable mobility degradation: $t_{ch}=10$ nm $\Rightarrow \mu_e=13,500$ cm$^2$/V.s

$t_{ch}=5$ nm $\Rightarrow \mu_e=9,950$ cm$^2$/V.s

Kim, IPRM 2010
Channel strain engineering

InAs 300 K quantum-well mobility vs. lattice constant:

Independent control of channel strain and composition:
→ new possibilities for channel design
THz HEMTs: possible designs

Etched S/D QW-MOSFET

Regrown S/D QW-MOSFET

FinFET

Gate-all-around nanowire FET
Conclusion

• THz HEMTs just around the corner

• Expanding interest on III-V CMOS: huge opportunity for THz HEMT electronics
  → fast technology progress
  → new processes and tools
  → fundamental research on transport, etc.
  → Si as substrate for THz electronics