InAs Quantum-Well MOSFET (L_g = 100 nm) with Record High g_m, f_T and f_max


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Abstract: This paper reports InAs quantum-well (QW) MOSFETs with record transconductance (g_m,max = 1.73 mS/μm) and high-frequency performance (f_T = 245 GHz and f_max = 355 GHz) at L_g = 100 nm. This record performance is achieved by using a low D_a composite Al2O3/InP gate stack, optimized layer design and a high mobility InAs channel. This work is significant because it shows a possible III-V material pathway from InAs/GaAs to InAs with similar processing and generalized characterization, including D_a.

Introduction: III-V semiconductors have emerged as a promising channel material for future CMOS low power logic applications [1-2]. Their enhanced electron transport properties offer significant power reduction through aggressive supply power (VDD) scaling. To maximize VDD scaling for logic application, both transconductance (g_m,ext) and subthreshold slope (S) must be optimized. We report 3 significant advances towards these goals: first an InAs sub channel to improve carrier transport property, second an optimized gate stack process with thin EOT of 2 nm and low D_a to improve S, and third an improved layer structure with thin InP barrier (to reduce access resistance) and optimized Si δ-doping (to improve S and reduce R_SD).

Experimental: Fig. 1 shows a cross-section of the device structure and Fig. 2 a corresponding TEM image of L_g = 100 nm device. A thin 2 nm InP barrier was used to reduce access resistance and improve charge control, EOT and immunity to short-channel effects as well as to improve D_a [3]. A 10 nm In0.53Ga0.47As/InAs/In0.53Ga0.47As composite channel with inverted Si δ-doping was chosen to improve carrier transport and electron confinement in the channel. Inverted Si δ-doping 5 nm below the channel inside the InAlAs buffer was used to supply carriers to the S/D access region and reduce R_SD without adding to the barrier thickness and EOT. It is critical to carefully select the inverted Si δ-doping density to achieve the best trade-off of threshold voltage (V_T), subthreshold slope (S) and parasitic resistance (R_SD).

Fig. 3 shows channel carrier density as a function of gate potential for various Si δ-doping densities. The ability to modulate the channel charge degrades as Siδ-doping increases, indicating that Si δ-doping needs to be carefully optimized for acceptable subthreshold characteristics [4]. In this work, we selected δ-doping = 1x10^{12} cm^-2, which resulted in both low R_SD (enabling record high g_m) and excellent electrostatic control (enabling good S). Fig. 4 shows the corresponding conduction band profile with Si δ-doping = 1x10^{12} cm^-2 at VDS = 0 V. In a calibration sample, we measured μ_Hall = 11,200 cm^2/V-sec and n_e,ch = 9 x 10^{15} cm^-3 at 300 K.

Device fabrication was similar to that of a conventional HEMT [4], with the addition of gate oxidation deposition prior to metal gate formation (3 nm of Al2O3 for an EOT = 2 nm). Additionally, MOS capacitors were fabricated with a thicker 10 nm Al2O3/InGaAs to enable accurate interfacial state density (Dϰ) extraction.

Results and Discussion: Fig. 5 shows MOSCAP C-V characteristics from 1 kHz to 1 MHz with low frequency dispersion in both accumulation and depletion. Analysis of the interfacial state density (Dϰ) was performed using the SEMATECH generalized technique [5] that combines High-Low frequency and Terman D_a extraction methods. This technique is a significant improvement on previous methods as it allows D_a, trap energy (E_T) and oxide capacitance (C_ox) to be determined simultaneously.

Fig. 6 shows excellent agreement between model and measured data, confirming the accuracy of the D_a result. Fitting the model simultaneously to the high frequency C-V (25 °C) and low frequency C-V (100 °C in order to accelerate trap response) curves produces the D_a vs. E_T dependence (Fig. 6, inset). D_a is lower in the upper portion of the band gap (minimum D_a = 4 x 10^{12} /eV-cm^2), which is preferable for NMOS device operation.

Fig. 7 shows the device output characteristics, demonstrating excellent pinch off and low R_SD (323 Ohm-µm). Fig. 8 shows typical subthreshold characteristics with excellent subthreshold behavior and Ion/Ioff ratio ~ 2 x 10^4 down to L_g = 100 nm. The gate leakage (I_g) is lower than 0.1 nA/µm at all measured bias conditions. InAs QW device with L_g = 100 nm exhibits V_T = +0.2 V (defined at I_D = 1µA/µm) and S = 105 mV/dec at VDS = 0.5 V. This results in an Ioff = 5 x 10^{4} A/µm at VDS = 0 V and VDS = 0.5 V. The attainment of this Ioff value in a device with low resistance parasitics and excellent subthreshold slope is significant because this is the first time that these three features are shown in combination in a III-V MOSFET. Fig. 9 shows good immunity to short-channel effects with controlled V_T roll-off at VDS = 50 mV and VDS = 0.5 V. Fig. 10 shows typical transconductance characteristics at VDS = 0.5 V. The InAs QW MOSFET exhibits g_m,max > 1.73 mS/µm at VDS = 0.5 V. This is a record transconductance for a III-V MOSFET of this gate length and V_T and it is the result of both the optimized Si δ-doping density that contributes to reduced access resistance and the high electron mobility associated with the InAs subchannel.

Microwave performance was characterized from 0.5 GHz to 50 GHz. Fig. 11 plots h21, U_A and stability-factor (k) against frequency. We obtained a current-gain cut-off frequency f_T = 245 GHz and a maximum oscillation frequency f_max = 355 GHz. These are record values for any III-V MOSFET. The device also exhibits f_T = 238 GHz at VDS = 0.5 V. Small-signal parameter extraction from measured S-parameters gave good consistency between DC and RF transconductance.

We benchmarked our devices with other state-of-the-art III-V MOSFETs (including surface, buried-channel and non-planar devices) using the figure of merit Q = g_m/S [6], as shown in Fig. 12 [7-11]. Our devices exhibit excellent transconductance and subthreshold slope with Q ~ 16, which can only be achieved with optimized layer structure, ohmic contacts (low R_SD) and low D_a / EOT gate-stack.

Conclusions: We have demonstrated quantum-well InAs MOSFETs with outstanding logic characteristics (S = 105 mV/dec, V_T = 0.2 V, Ioff = 5x10^{4} A/µm and g_m,max > 1.73 mS/µm at VDS = 0.5 V). In addition, our devices show record f_T = 245 GHz and f_max = 355 GHz. These results emerge from an optimized layer structure (with thin InP barrier and inverted Si δ-doping), high quality Al2O3/InP gate stack, and high mobility InAs channel.
Fig. 1: Cross-sectional schematic of QW device with 3 nm ALD Al₂O₃, 2 nm InP barrier and InAs composite channel.

Fig. 2: TEM cross-section of fabricated device. Note well optimized recess with minimal Lₘᵦᵣₜₜₜ.

Fig. 3: 1d Poisson-Schrödinger simulations of channel electron density as a function of gate bias. High δ-doping density limits charge modulation.

Fig. 4: 1d Poisson-Schrödinger simulation of conduction band profile and electron wave-function for the optimized Si δ-doping condition.

Fig. 5: Room temperature CV characteristics of partner In₀.₅₃Ga₀.₄₇As MOSCAP with 10 nm ALD Al₂O₃ (reduced leakage for accurate CV measurement).

Fig. 6: Measured and simulated CV curves with inset of Dᵦ extracted using the generalized technique as a function of energy. Note mid-gap Dᵦ of ~4x10¹² eV·cm⁻².

Fig. 7: Iᵥₐₗₜ output characteristics showing excellent charge control and low series resistance (323 Ω·µm).

Fig. 8: Semi-log scale Iᵥₐₗₜ versus Vᵥₑₜ for the optimized Si δ-doping condition.

Fig. 9: Vᵥₑₜ versus Lₑₜ. Devices display excellent immunity to Vᵥₑₜ roll-off given EOT of 2 nm and buried channel design.

Fig. 10: Microwave characteristics of Lₑₜ = 100 nm InAs MOSFET with the highest fₜ = 245 GHz and fₘₐₓ = 355 GHz of any III-V MOSFET.

Fig. 11: Microwave characteristics of Lₑₜ = 100 nm InAs MOSFET with the highest fₜ = 245 GHz and fₘₐₓ = 355 GHz of any III-V MOSFET.

Fig. 12: gₑₘₐₓ versus Q or quality factor. This work has state of the art performance with record gₑₘₐₓ for a given gate length.