III-V High-Electron Mobility Transistors on the path to THz operation

J. A. del Alamo¹ and D.-H. Kim²

¹Microsystems Technology Laboratories, MIT
²Previously with Teledyne Scientific, now with Global Foundries

International Conference on Solid State Devices and Materials
Kyoto, Sept. 25-27, 2012

Acknowledgements: Jianqiang Lin, Tae-Woo Kim, Niamh Waldron
Sponsors: FCRP-MSD, Intel, SRC, ARL
Labs at MIT: MTL, SEBL, NSL
Outline

1. High-frequency III-V HEMTs: megatrends
2. State-of-the-art InGaAs HEMTs and $f_T$ analysis
3. The path to THz operation
1. III-V HEMT: record $f_T$ vs. time

- For >20 years, record $f_T$ obtained on InGaAs-channel HEMTs
- InGaAs-channel HEMTs offer record balanced $f_T$ and $f_{\text{max}}$

Current record:
- $f_T=688$ GHz
- $f_{\text{max}}=800$ GHz
- Kim IEDM 2011 (Teledyne/MIT)
Record $f_T$ III-V HEMTs: megatrends

- Over time: $L_g \downarrow$, $\ln_x \text{Ga}_{1-x}\text{As}$ channel $x_{\ln\text{As}} \uparrow$
- $L_g$, $x_{\ln\text{As}}$ saturated $\rightarrow$ no more progress possible?
Record $f_T$ III-V HEMTs: megatrends

- Over time: $t_{ch} \downarrow$, $t_{ins} \downarrow$
- $t_{ch}$, $t_{ins}$ saturated $\rightarrow$ no more progress possible?
2. State-of-the-art InGaAs HEMT

$L_g = 40$ nm InGaAs MHEMT

- In$_{0.7}$Ga$_{0.3}$As QW channel
  - $t_{ch} = 10$ nm
  - $\mu_{n,Hall} > 10,000$ cm$^2$/V-sec
- In$_{0.52}$Al$_{0.48}$As barrier + In$_{0.7}$Al$_{0.3}$As spacer (Kim, EL 2011)
- Dual Si $\delta$-doping (Kim, IEDM 2010)
- Pt (3 nm)/Ti/Pt/Au Schottky
  - $t_{ins} = 4$ nm
- InP etch stop ($t_{InP} = 6$ nm)
- $L_{side} = 100$ nm
- Gate stem > 250 nm
- Mo-based S/D with 2 $\mu$m S-D spacing

Kim, IEDM 2011
TEM cross section
Output and transfer characteristics

- Large current drive: $I_D > 1 \text{ mA/µm}$ at $V_{DS} = 0.8 \text{ V}$
- High transconductance: $g_{mpk} = 2.75 \text{ mS/µm}$ at $V_{DS} = 0.8 \text{ V}$
- $V_T \approx 0 \text{ V}$, $R_{ON} = 280 \Omega \cdot \mu m$

Kim, IEDM 2011

---

![Graphs showing output and transfer characteristics for L_g=40 nm. The graphs illustrate the relationship between $I_D$ and $V_{DS}$ at $V_{GS} = 0.6 \text{ V}$, and $g_m$ and $V_{GS}$ at $V_{DS} = 0.1 \text{ V}$ and $0.8 \text{ V}$.](image-url)
High-frequency characteristics

- Only transistor of any kind with both $f_T$ and $f_{max} > 680$ GHz
- Obtained at same bias point, $V_{DS}=0.6$ V

Kim, IEDM 2011
\[ f_T \text{ vs. } f_{\text{max}} \]

\[ f_{\text{avg}} = \sqrt{f_T f_{\text{max}}} \]

- Record \( f_T \) FET
- Best-balanced \( f_T \) and \( f_{\text{max}} \) transistor

Kim, IEDM 2010
\( f_{\text{max}} = 1.25 \text{ GHz} \)

Kim, IEDM 2011
**f<sub>t</sub> analysis**

- First-order $f_T$ expression for HEMT:

$$f_T = \frac{1}{2\pi} \frac{g_{mi}}{C_{gs} + C_{gd} + g_{mi}(R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]}$$
Break out extrinsic capacitances

- Capacitance components:

\[
C_{gs} = C_{gsi} + C_{gsext} \quad \quad \quad \quad \quad C_{gd} = C_{gdi} + C_{gdext}
\]
Delay time analysis

• Delay time:

\[ \tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par} \]

• Components of delay time:

- Intrinsic delay (transit time)

\[ \tau_t = \frac{C_{gs} + C_{gdi}}{g_{mi}} = \frac{L_g}{< v_e >} \]

- Extrinsic delay

\[ \tau_{ext} = \frac{C_{gs} + C_{gd}}{g_{mi}} \]

- Parasitic delay

\[ \tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd}) \frac{g_{oi}}{g_{mi}}] \]
Delay components of $L_g=40$ nm InGaAs HEMT

Delay time from $f_T$: ~231 fs
- Intrinsic delay: ~81 fs
- Extrinsic delay: ~99 fs
- Parasitic delay: ~50 fs
- Unaccounted: ~9 fs

yields $<v_e> = 5 \times 10^7$ cm/s

most significant
Scaling of delay components

$$\tau_{\text{ext}}$$ and $$\tau_{\text{par}}$$ do not scale, become dominant for $$L_g < 50 \text{ nm}$$

- $$V_{DS} = 0.6 \text{ V}$$
- $$V_{GS} - V_T = 0.3 \text{ V}$$
Scaling of small-signal components

As $L_g \downarrow$:

- $g_{mi}$ does not scale
- $g_{oi}$ does not scale

$$\tau_{ext} = \frac{C_{gs, ext} + C_{gd, ext}}{g_{mi}}$$

$$\tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]$$
3. The path to THz operation

- **Intrinsic delay** ↓ → \( L_g \) ↓

- **Extrinsic delay** ↓:
  \[
  \tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}
  \]
  → \( C_{gsext}, C_{gdext} \) ↓ → gate engineering
  → \( g_{mi} \) ↑ → harmonious scaling

- **Parasitic delay** ↓:
  \[
  \tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]
  \]
  → \( R_S + R_D \) ↓ → S/D engineering
  → \( g_{oi}/g_{mi} \) ↓ → harmonious scaling
How to reach $f_T = 1$ THz?

$f_T = 1$ THz feasible by:

→ scaling to $L_g \approx 25$ nm

→ ~30% parasitic reduction
Approach to \( R_s + R_D \downarrow \): self-aligned process

- Dry-etched Mo contacts: \( R_c = 7 \ \Omega \cdot \mu m \)
- \( L_g = 50 \ \text{nm}, \ R_{ON} = 290 \ \Omega \cdot \mu m, \ g_{mpk} = 2.2 \ \text{mS/\mu m} @ V_{DS} = 0.5 \ \text{V} \)

Kim, IEDM 2010
Waldron, TED 2010

L_{side} = 100 \ \text{nm}
L_g=60 nm self-aligned In_{0.7}Ga_{0.3}As HEMT

- f_T = 595 GHz
- f_max = 680 GHz

Kim, IEDM 2010

Highest f_T and f_max of any FET at L_g ≥ 60 nm
$L_g=30\text{ nm}$ self-aligned InGaAs MOSFET with $L_{\text{side}}\sim30\text{ nm}$

Lin, IEDM 2012

![MOSFET image]

$g_{mpk}=1.4\text{ mS/\mu m}$

$R_{\text{ON}}=475\text{ \Omega.\mu m} \rightarrow$ access region design critical!
Regrown source and drain regions

$L_{ch} = 55 \text{ nm InGaAs MOSFET:}$
$R_{ON} = 199 \, \Omega \mu m$
Egard, IEDM 2011

$L_{ch} = 30 \text{ nm InGaAs MOSFET:}$
$R_{ON} = 133 \, \Omega \mu m$
Zhou, EDL 2012
Harmonious scaling: aspect ratio of record $f_t$ devices

- Channel AR: 3 ~ 4
- Insulator AR: 7 ~ 10

For $L_g$=25 nm
\[ t_{ch} \sim 7 \text{ nm}, \ t_{ins} \sim 3 \text{ nm} \]
Limit to HEMT barrier scaling: gate leakage current

InAlAs/InGaAs HEMTs

At $L_g=30$ nm, modern HEMTs are at the limit of scaling!
Limit to HEMT barrier scaling: gate leakage current

InAlAs/InGaAs HEMTs

$V_{DS} = 0.5 \, \text{V}$

$V_{GS} \text{ [V]}$

$I_G \text{ [A/\mu m]}$

$t_{\text{ins}} = 2 \, \text{nm}$

$t_{\text{ins}} = 4 \, \text{nm}$

$t_{\text{ins}} = 7 \, \text{nm}$

$t_{\text{ins}} = 10 \, \text{nm}$

$10^{-5} \times$

Al$_2$O$_3$ (3 nm)/InP (2 nm)/InGaAs MOSFET

Need high-K gate dielectric: HEMT $\rightarrow$ MOSFET!
III-V MOSFET: deep scaling possible

InP (1 nm) + Al₂O₃ (0.4 nm) + HfO₂ (2 nm) $\rightarrow$ EOT $\sim$ 0.9 nm
[vs. 4 nm InAlAs $\rightarrow$ EOT = 1.3 nm]
$\rightarrow$ should bring us to $L_g=20$ nm

Long-channel
In₀.₅₃Ga₀.₄₇As MOSFET
$\mu_e \approx 2700$ cm²/V.s

Lin, IEDM 2012

S=69 mV/dec $\rightarrow$ Low $D_{it}$ at MOS interface demonstrated
High-frequency InGaAs MOSFETs

$L_g=100$ nm InGaAs MOSFET with $L_{side} \sim 5$ nm, $EOT=1.9$ nm

$\mu_e=4600$ cm$^2$/V.s

$f_t=245$ GHz, $R_{ON}=323$ $\Omega$.µm, $g_m=1.7$ mS/µm, $S=105$ mV/dec
THz MOSFETs: possible designs

- Etched S/D QW-MOSFET
- Regrown S/D QW-MOSFET
- FinFET
- Gate-all-around nanowire FET
Conclusions

• THz III-V FETs just around the corner
  → need to reduce parasitics
  → need to scale harmoniously

• Exploding interest on III-V CMOS: huge opportunity for THz III-V electronics!
  → fast technology progress
  → new processes and tools
  → fundamental research on transport, interface, etc.
  → Si as substrate for THz electronics