Sub-30 nm InAs Quantum-Well MOSFETs
with Self-Aligned Metal Contacts and
Sub-1 nm EOT HfO$_2$ Insulator

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Motivation

- Superior electron transport properties in InAs and InGaAs material systems
  - ~10X mobility vs. Silicon
  - Extraordinary electron velocity

\[ I_{d-sat} = Q_{i_xo} \times v_{inj} \]

[InAs HEMTs]

\[ V_{DS}=0.5 \text{ V} \]

\[ V_{DS}=1.1-1.3 \text{ V} \]
Goal: Self-aligned III-V QW-MOSFETs

- Deeply scaled channel and barrier
- Architecture: Self-aligned contact
- Process integration: towards Si-MOS-compatible processes and materials
Device fabrication

- **SiO₂**
- **Mo**
- **n⁺ cap**
- **i-InP**
- **Channel**
- **δ-Si**
- **Buffer**
- **InP substrate**

- Sputtered Mo contact
- CVD SiO₂ hard mask
- Mesa isolation
Device fabrication

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- Gate lithography
- Gate recess by RIE SiO₂/Mo
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- Damage annealing *
- Cap wet etch; Mo pulled-in
- Digital etching of InP

* [Lin, APEX 2012]
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- Mo gate evaporation
- Gate head photo and pattern
- Pad formation
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- Self-aligned
- InP exposed last
- Low thermal budget

- Au-free (Front-end)
- Lift-off free (Front-end)
QW-MOSFET: $L_g=30$ nm

- Channel (total $t_{ch}=10$ nm): 2 nm InAs clad by 3 and 5 nm In$_{0.7}$Ga$_{0.3}$As
- InP barrier thinned by digital etch
- Barrier InP =1 nm, HfO$_2$ =2 nm [including barrier: EOT~ 0.8 nm]
- Low-$\rho$ Mo: $t_{Mo,S/D}=30$ nm, $R_{sh}=5 \ \Omega/\square$
- Contact to gate spacing $= 20$~30 nm
QW-MOSFET: $L_g=30$ nm

- $g_{m,\text{max}} = 1.4 \text{ mS/\text{	extmu m}}$ at $V_{DS}=0.5 \text{ V}$
- Little hysteresis ($< 10 \text{ mV}$)
- $R_{on}=470 \text{ \Omega}.\mu\text{m}$, $R_{sd}=450 \text{ \Omega}.\mu\text{m}$ (mainly attributed to $L_{\text{side}}$)
**QW-MOSFET:** $L_g = 30$ nm

**Subthreshold characteristic**

- $S_{\text{min}} = 114$ mV/dec at $V_{DS} = 0.5$ V, DIBL = 230 mV/V
- Nearly constant $S$ throughout subthreshold region
- $I_g < 1$ nA/µm over entire voltage range
Scaling and benchmarking: ON current

- Superior behavior to any planar III-V MOSFET to date
- Matches performance of III-V Trigate MOSFETs [Radosavljevic, IEDM 2011]
Scaling and benchmarking: Subthreshold swing and $V_t$ roll-off

- $S_{\min}$ superior to all planar III-V MOSFETs to date
- Matches III-V Trigate MOSFET [Radosavljevic, IEDM 2011]
- $V_t$ roll-off starts at $L_g \sim 50$ nm
• DIBL = 230 mV/V for $L_g=30$ nm
• Related to residual RIE damage and the heterostructure
QW-MOSFET: \( L_g = 22 \) nm

- Functional device with \( L_g = 22 \) nm
- \( g_{m, \text{max}} = 1.1 \) mS/\( \mu \)m at \( V_{DS} = 0.5 \) V
Dielectric/barrier scaling

Long-channel In$_{0.53}$Ga$_{0.47}$As QW-MOSFET

- Fresh InP surface exposed right before high-k deposition
- $\text{Al}_2\text{O}_3$ (0.4 nm) + $\text{HfO}_2$ (2 nm) [EOT of deposited insulator layer $\sim$0.6 nm]
- InP thinned to $\sim$ 1 nm [Gate-Channel EOT$\sim$0.9 nm]
Benchmarking: Long-channel subthreshold swing on planar MOSFETs

- Close to lowest $S_{\text{min}}$ reported in any III-V MOSFET: 66 mV/dec [EOT=1.2 nm] [Radosavljevic, IEDM 2011]

![Graph showing subthreshold swing vs EOT of dielectric]
HfO$_2$ vs. Al$_2$O$_3$

Recent study at U. Texas at Dallas:

- HfO$_2$ on InP yields lower D$_{it}$ than Al$_2$O$_3$
HfO$_2$ vs. Al$_2$O$_3$

- Split C-V measurement on $L_g = 20 \ \mu m$
- Lower dispersion for HfO$_2$ below threshold
First demonstration of HfO$_2$ directly on InP for InAs QW-MOSFET
- Steeper subthreshold swing at $L_g=150$ nm at low $V_{GS}$
- Lower EOT
Mobility in Long QW-MOSFETs

- Mobility extracted by split C-V method
- \( N_s \) not corrected by \( D_{it} \)
- Channel design beneficial to maintain high mobility:
  - Undoped channel
  - InAs-rich channel
  - Buried-channel design

4650 cm\(^2\)V\(^{-1}\)s\(^{-1}\) at \( N_s = 4 \times 10^{12} \) cm\(^{-2}\)

\( \mu_e \) (cm\(^2\)V\(^{-1}\)s\(^{-1}\))

\( N_s \) (x10\(^{12}\) cm\(^{-2}\))

- \( \mu_e \) for \( \text{HfO}_2 \) (2 nm) and \( \text{Al}_2\text{O}_3 \) (2 nm)

\( L_g = 20 \) \( \mu \)m

Mo Gate
High-k
i-InP (1 nm)
Channel (10 nm):
InGaAs/InAs/InGaAs (3/2/5 nm)
\( \delta \)-Si
Buffer
Conclusions

• Novel self-aligned gate-last MOSFET architecture:
  – Self-aligned gate to contact metals ($L_{\text{side}} \sim 20-30$ nm)
  – Improved Si-MOS process compatibility
  – Fresh InP surface exposed right before high-k deposition
  – Deeply scaled dielectric

• Outstanding performance and short-channel effects in devices with $L_g = 30$ nm

• Demonstrated subthreshold swing of 69 mV/dec and mobility of 4650 cm$^2$V$^{-1}$s$^{-1}$ at $N_s = 4 \times 10^{12}$ cm$^{-2}$ in long channel QW-MOSFETs

• HfO$_2$ / InP dielectric for superior performance
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