THz III-V HEMT Technology

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International Wireless Symposium 2013
Workshop on THz Material Growth, Device Fabrication and Modeling
Beijing, April 14, 2013

Acknowledgements: Dae-Hyun Kim, Jianqiang Lin, Tae-Woo Kim, Niamh Waldron
Sponsors: FCRP-MSD, Intel, SRC, ARL
Labs at MIT: MTL, SEBL, NSL
Outline

1. High-frequency III-V HEMTs: megatrends
2. State-of-the-art InGaAs HEMTs and $f_T$ analysis
3. The path to THz operation
• For >20 years, record $f_T$ obtained on InGaAs-channel HEMTs
• InGaAs-channel HEMTs offer record balanced $f_T$ and $f_{\text{max}}$
Record $f_T$ III-V HEMTs: megatrends

- Over time: $L_g \downarrow$, $\ln_x \text{Ga}_{1-x} \text{As}$ channel $x_{\ln\text{As}} \uparrow$
- $L_g$, $x_{\ln\text{As}}$ saturated $\Rightarrow$ no more progress possible?
Record $f_T$ III-V HEMTs: megatrends

- Over time: $t_{ch} \downarrow$, $t_{ins} \downarrow$
- $t_{ch}$, $t_{ins}$ saturated $\rightarrow$ no more progress possible?
2. State-of-the-art InGaAs HEMT

$L_g = 40$ nm InGaAs Metamorphic HEMT

- $\text{In}_0.7\text{Ga}_{0.3}\text{As}$ QW channel
  - $t_{\text{ch}} = 10$ nm
  - $\mu_{n,\text{Hall}} > 10,000$ cm$^2$/V-sec
- $\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ barrier + $\text{In}_{0.7}\text{Al}_{0.3}\text{As}$ spacer (Kim, EL 2011)
- Dual Si $\delta$-doping (Kim, IEDM 2010)
- Pt (3 nm)/Ti/Pt/Au Schottky
  - $t_{\text{ins}} = 4$ nm
- InP etch stop ($t_{\text{InP}} = 6$ nm)
- $L_{\text{side}} = 100$ nm
- Gate stem $> 250$ nm
- Mo-based S/D with 2 $\mu$m S-D spacing
TEM cross section

GaAs Substrate
Graded Buffer
HEMT Epi
Buried Pt
Ti
Pt
Au

S
G
D

0.5 μm

20 nm

Buried Pt
Output and transfer characteristics

- Large current drive: $I_D > 1 \text{ mA/\mu m}$ at $V_{DS} = 0.8 \text{ V}$
- High transconductance: $g_{mpk} = 2.75 \text{ mS/\mu m}$ at $V_{DS} = 0.8 \text{ V}$
- $V_T \approx 0 \text{ V}$, $R_{ON} = 280 \Omega .\mu m$
• Only transistor of any kind with both $f_T$ and $f_{\text{max}} > 680$ GHz
• Obtained at same bias point, $V_{DS}=0.6$ V

Kim, IEDM 2011
**f_T vs. f_max**

\[
f_{\text{avg}} = \sqrt{f_T f_{\text{max}}}
\]

- Record \( f_T \) FET
- Best-balanced \( f_T \) and \( f_{\text{max}} \) transistor

Kim, IEDM 2010
\((f_{\text{max}}=1.25 \text{ GHz})\)

Kim, IEDM 2011

MIT/TSC HEMT
Fujitsu HEMT
NGAS HEMT
SNU HEMT
UCSB HBT
UIUC HBT
TSC HBT
HRL HBT
ETH HBT
• First-order $f_T$ expression for HEMT:

$$f_T = \frac{1}{2\pi} \frac{g_{mi}}{C_{gs} + C_{gd} + g_{mi}(R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]}$$
Break out extrinsic capacitances

- Capacitance components:

\[ C_{gs} = C_{gsi} + C'_{gsext} \quad \quad C'_{gd} = C'_{gdi} + C_{gdext} \]
Delay time analysis

- Delay time:
  \[ \tau = \frac{1}{2\pi f_T} = \tau_t + \tau_{ext} + \tau_{par} \]

- Components of delay time:
  \[ \tau_t = \frac{C_{gsi} + C_{gdi}}{g_{mi}} = \frac{L_g}{\langle v_e \rangle} \]
  Intrinsic delay (transit time)

  Extrinsic delay

  \[ \tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}} \]

  Parasitic delay

  \[ \tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd}) \frac{g_{oi}}{g_{mi}}] \]
Extraction of parasitic capacitances

- Need devices with different $L_g$
- Bias them at same $V_{GS}$ overdrive around peak $f_T$ point
- Extract small-signal equivalent circuit models
- Study $L_g$ scaling behavior of $C_{gs}$ and $C_{gd}$

\[\begin{align*}
V_{DS} &= 0.6 \text{ V} \\
V_{GS} - V_T &= 0.3 \text{ V}
\end{align*}\]

Kim, IEDM 2011
Delay components of \( L_g = 40 \) nm InGaAs HEMT

- Delay time from \( f_T \): \( \sim 231 \) fs
  - Intrinsic delay: \( \sim 81 \) fs
  - Extrinsic delay: \( \sim 99 \) fs
  - Parasitic delay: \( \sim 50 \) fs
  - Unaccounted: \( \sim 9 \) fs

\[ \langle v_e \rangle = 5 \times 10^7 \text{ cm/s} \]

Most significant delay component is extrinsic delay, \( \sim 99 \) fs.

Kim, IEDM 2011
Scaling of delay components

\[ \tau_{ext} \text{ and } \tau_{par} \text{ do not scale, become dominant for } L_g < 50 \text{ nm} \]
Scaling of small-signal components

As $L_g \downarrow$:

- $g_{mi}$ do not scale
- $g_{oi}$ do not scale
- $\tau_{ext} = \frac{C_{gs_{ext}} + C_{gd_{ext}}}{g_{mi}}$
- $\tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]$
3. The path to THz operation

- **Intrinsic delay** ↓ → \( L_g \) ↓
- **Extrinsic delay** ↓:
  \[
  \tau_{ext} = \frac{C_{gsext} + C_{gdext}}{g_{mi}}
  \]
  → \( C_{gsext}, C_{gdext} \) ↓ → gate engineering
  → \( g_{mi} \) ↑ → harmonious scaling
- **Parasitic delay** ↓:
  \[
  \tau_{par} = (R_S + R_D)[C_{gd} + (C_{gs} + C_{gd})\frac{g_{oi}}{g_{mi}}]
  \]
  → \( R_S + R_D \) ↓ → S/D engineering
  → \( g_{oi}/g_{mi} \) ↓ → harmonious scaling
How to reach $f_T = 1$ THz?

- Scaling to $L_g \approx 25$ nm
- $\sim 30\%$ parasitic reduction

30% reduction in all the parasitics
Approach to $R_S + R_D$: self-aligned process

- Dry-etched Mo contacts: $R_c = 7 \, \Omega \cdot \mu m$
- $L_g = 50 \, \text{nm}$, $R_{ON} = 290 \, \Omega \cdot \mu m$, $g_{mpk} = 2.2 \, \text{mS/\mu m} \, \text{at} \, V_{DS} = 0.5 \, \text{V}$
L_g = 60 nm self-aligned In_{0.7}Ga_{0.3}As HEMT

Kim, IEDM 2010

Highest f_T and f_max of any FET at L_g ≥ 60 nm

L_g = 60 nm

Measured data
Modeled data

V_{GS} = 0.2 V, V_{DS} = 0.6 V

f_T = 595 GHz
f_max = 680 GHz
Lg=30 nm self-aligned InGaAs MOSFET with Lside~30 nm

Lin, IEDM 2012

\[ g_{mpk} = 1.4 \text{ mS/\mu m} \]

\[ R_{ON} = 475 \Omega \cdot \mu m \rightarrow \text{access region design critical!} \]
Regrown source and drain regions

\( L_{ch} = 55 \text{ nm InGaAs MOSFET:} \)
\( R_{ON} = 199 \ \Omega \mu \text{m} \)

Egard, IEDM 2011

\( L_{ch} = 30 \text{ nm InGaAs MOSFET:} \)
\( R_{ON} = 133 \ \Omega \mu \text{m} \)

Zhou, EDL 2012
Harmonious scaling: aspect ratio of record $f_t$ devices

Channel Aspect Ratio: $L_g/t_{ch}$
Insulator Aspect Ratio: $L_g/t_{ins}$

- **Channel AR**: $3 \sim 4$
- **Insulator AR**: $7 \sim 10$

For $L_g=25$ nm:

$\rightarrow t_{ch} \sim 7$ nm, $t_{ins} \sim 3$ nm
Issues in channel scaling

Deep channel thickness scaling degrades performance:

$\Rightarrow R_s \uparrow \Rightarrow f_T \downarrow$

Noticeable mobility degradation:

$t_{ch} = 10 \text{ nm} \Rightarrow \mu_e = 13,500 \text{ cm}^2/\text{V.s}$

$t_{ch} = 5 \text{ nm} \Rightarrow \mu_e = 9,950 \text{ cm}^2/\text{V.s}$

Kim, IPRM 2010
**V\text{inj} - impact of channel thickness**

In thin-channel devices:
- Long \(L_g\): \(V_{\text{inj}}\) decreases right along with \(\mu_e\) (~23%)
- Short \(L_g\): \(V_{\text{inj}}\) relatively unaffected
  \(\rightarrow\) consistent with near ballistic transport

\[ V_{DS} = 0.5 \text{ V} \]

\[ \mu_n \sim 13,000 \text{ cm}^2/\text{V-s} \]
\[ t_{\text{ins}} = 4 \text{ nm} \& t_{\text{ch}} = 10 \text{ nm} \]

\[ \mu_n \sim 9,950 \text{ cm}^2/\text{V-s} \]
\[ t_{\text{ins}} = 3 \text{ nm} \& t_{\text{ch}} = 5 \text{ nm} \]

Strain-Si

Si nFETs

(V\(_{DS}\) = 1.1 ~ 1.3 V)

Kim, IEDM 2009

\[ V_{\text{inj}} \left[10^7 \text{ cm/s}\right] \]

\[ L_g \left[\text{nm}\right] \]
Channel transport enhancement through strain engineering

InAs 300 K quantum-well mobility vs. lattice constant:

Independent control of channel strain and composition: → new possibilities for channel design
Issues in barrier scaling

Want to scale $L_g$ without degrading $g_m$ or $g_o$

For harmonious scaling: as $L_g \downarrow \rightarrow t_{ins} \downarrow$

$\text{In}_{0.7}\text{Ga}_{0.3}\text{As HEMTs}$
$t_{ch}=13\ \text{nm},\ L_{side}=150\ \text{nm}$

$V_{DS}=0.5\ \text{V}$

Kim, TED 2008
Limit to HEMT barrier scaling: gate leakage current

At $L_g=40$ nm, modern HEMTs are at the limit of scaling!
Limit to HEMT barrier scaling: gate leakage current

InAlAs/InGaAs HEMTs

$V_{DS}=0.5$ V
$L_g=40$ nm

$V_{GS}$ [V]

$I_G$ [A/μm]

$10^{-4}$
$10^{-6}$
$10^{-8}$
$10^{-10}$
$10^{-12}$
$10^{-14}$

$V_{DS}=0.5$ V
$V_{GS}$ [V]
$t_{\text{ins}} = 2$ nm
$t_{\text{ins}} = 4$ nm
$t_{\text{ins}} = 7$ nm
$t_{\text{ins}} = 10$ nm

$10^{-5} \times$!

Need high-K gate dielectric: HEMT $\rightarrow$ MOSFET!
III-V MOSFET: deep scaling possible

InP (1 nm) + Al₂O₃ (0.4 nm) + HfO₂ (2 nm) → EOT ~ 0.9 nm
[vs. 4 nm InAlAs → EOT = 1.3 nm]
→ should bring us to L₉ = 20 nm

Long-channel
In₀.₅₃Ga₀.₄₇As MOSFET
μₑ ≈ 2700 cm²/V.s

S=69 mV/dec → Low Dᵢ₊ at MOS interface demonstrated

Lin, IEDM 2012
High-frequency InGaAs MOSFETs

$L_g = 60 \text{ nm}$ InGaAs MOSFET with $L_{\text{side}} \sim 5 \text{ nm}$, EOT=1.2 nm

Kim, APL 2012

$f_t = 370 \text{ GHz}$, $R_{\text{ON}} = 220 \Omega \cdot \mu \text{m}$,
$g_m = 2.0 \text{ mS/}\mu \text{m}$, $S = 110 \text{ mV/dec}$

$L_g = 60 \text{ nm}$
$V_{DS} = 0.5 \text{ V}$
THz MOSFETs: possible designs

Etched S/D QW-MOSFET

Regrown S/D QW-MOSFET

FinFET

Gate-all-around nanowire FET
Conclusions

• THz III-V FETs just around the corner
  → need to reduce parasitics
  → need to scale harmoniously

• Exploding interest on III-V CMOS: huge opportunity for THz III-V electronics!
  → fast technology progress
  → new processes and tools
  → fundamental research on transport, interface, etc.
  → Si as substrate for THz electronics