InGaAs Nanoelectronics:
from THz to CMOS

J. A. del Alamo
Microsystems Technology Laboratories, MIT

IEEE International Conference on Electron Devices and Solid-State Circuits
Hong Kong, June 3, 2013

Acknowledgements:
• Sponsors: Intel, FCRP-MSD
• Labs at MIT: MTL, NSL, SEBL
Outline

1. InGaAs HEMT today
2. InGaAs HEMTs towards THz operation
3. InGaAs MOSFETs: towards sub-10 nm CMOS
A bit of perspective...

- Invention of AlGaAs/GaAs HEMT: Fujitsu Labs. 1980
- First InAlAs/InGaAs HEMT on InP: Bell Labs. 1982
- First AlGaAs/InGaAs Pseudomorphic HEMT: U. Illinois 1985
- Main attraction of InGaAs: RT $\mu_e = 6,000\sim30,000$ cm$^2$/V.s

Mimura JJAPL 1980  
Chen EDL 1982  
Ketterson EDL 1985
InGaAs Electronics Today

UMTS-LTE PA module
Chow, MTT-S 2008

40 Gb/s modulator driver
Carroll, MTT-S 2002

77 GHz transceiver
Tessmann, GaAs IC 1999

Single-chip WLAN MMIC
Morkner, RFIC 2007

Bipolar/E-D PHEMT process
Henderson, Mantech 2007
InGaAs High Electron Mobility Transistor (HEMT)

Modulation doping:
→ 2-Dimensional Electron Gas at InAlAs/InGaAs interface
InGaAs HEMT: high-frequency record vs. time

- Highest $f_T$ of any FET on any material system
- Best balanced $f_T$ and $f_{max}$ of any transistor on any material

Teledyne/MIT: $f_T=688$ GHz, $f_{max}=800$ GHz

Devices fabricated at MIT

Chang APEX 2013 (NCTU)
InGaAs HEMTs: circuit demonstrations

10-stage 670 GHz LNA
Leong, IPRM 2012

Single-stage 500 GHz LNA
Sarkozy, IPRM 2013

80 Gb/s multiplexer IC
Wurfl, GAAS 2004

Tessmann, CSIC 2010
InGaAs HEMTs on InP used to map infant universe

WMAP = Wilkinson Microwave Anisotropy Probe
Launched 2001

Full-sky map of Cosmic Microwave Background radiation (oldest light in Universe) → age of Universe: 13.73B years (±1%)

http://map.gsfc.nasa.gov/

0.1 µm InGaAs HEMT LNA
Pospieszalski MTT-S 2000
A closer look: InGaAs HEMTs at MIT

- QW channel ($t_{ch} = 10$ nm):
  - InAs core
  - InGaAs cladding
  - $\mu_e = 13,200$ cm$^2$/V-sec
- InAlAs barrier ($t_{ins} = 4$ nm)
- $L_g = 30$ nm

Kim, EDL 2010
\( L_g = 30 \text{ nm InGaAs HEMT} \)

- High transconductance: \( g_m = 1.9 \text{ mS/\mu m at } V_{DD} = 0.5 \text{ V} \)
- First transistor of any kind with both \( f_T \) and \( f_{max} > 640 \text{ GHz} \)

Kim, EDL 2010
How to reach $f_T = 1$ THz?

$f_T = 1$ THz feasible by:

$\rightarrow$ scaling to $L_g \approx 25$ nm

$\rightarrow$ ~30% parasitic reduction

Kim, IEDM 2011
Record $f_T$ InGaAs HEMTs: megatrends

- Over time: $L_g \downarrow$, $x_{InAs}$ increases
- $L_g$, $x_{InAs}$ saturated $\rightarrow$ no more progress possible?
Record $f_T$ InGaAs HEMTs: megatrends

- Over time: $t_{ch}$, $t_{ins}$
- $t_{ch}$, $t_{ins}$ saturated → no more progress possible?
Limit to HEMT barrier scaling: gate leakage current

At $L_g=30-40$ nm, modern HEMTs are at the limit of scaling!
Solution: MOS gate!

Need high-K gate dielectric: HEMT $\rightarrow$ MOSFET!

Al$_2$O$_3$ (3 nm)/InP (2 nm)/InGaAs MOSFET

$L_g$=40 nm, $V_{DS}$=0.5 V

Kim, EDL 2013
InGaAs MOSFETs with $f_T = 370$ GHz  
(Teledyne/ MIT/ IntelliEpi/ Sematech)

Kim, APL 2012

- Channel: 10 nm In$_{0.7}$Ga$_{0.3}$As
- Barrier: 1 nm InP + 2 nm Al$_2$O$_3$
- $L_g = 60$ nm
- $g_m = 2$ mS/$\mu$m
- $R_{ON} = 220 \, \Omega \cdot \mu$m
III-V MOSFET: a >30 year pursuit!

Poor electrical characteristics due to oxide/semiconductor interface defects $\rightarrow$ Fermi level pinning

Kohn, EL 1977

Mimura, EL 1978
Recent breakthrough: oxide/III-V interfaces with unpinned Fermi level

*In-situ* UHV Ga$_2$O$_3$-Gd$_2$O$_3$ on GaAs

*Ex-situ* ALD Al$_2$O$_3$ on GaAs

Ren, SSE 1997

Ye, EDL 2003
“Self-cleaning” during ALD

ALD eliminates surface oxides that pin Fermi level:
- First observed with $\text{Al}_2\text{O}_3$, then with other high-K dielectrics
- First seen in GaAs, then in other III-Vs

Huang, APL 2005
Interface quality: \( \text{Al}_2\text{O}_3/\text{InGaAs} \) vs. \( \text{Al}_2\text{O}_3/\text{Si} \)

Close to conduction band edge, \( \text{Al}_2\text{O}_3/\text{InGaAs} \) shows comparable interface state density to \( \text{Al}_2\text{O}_3/\text{Si} \) interface.
Electron injection velocity: InGaAs vs. Si

Measurements of electron injection velocity in HEMTs:

- $v_{\text{inj}}(\text{InGaAs})$ increases with InAs fraction in channel
- $v_{\text{inj}}(\text{InGaAs}) > 2v_{\text{inj}}(\text{Si})$ at less than half $V_{\text{DD}}$
- ~100% ballistic transport at $L_g \sim 30$ nm
InGaAs n-MOSFET: best candidate for post-Si CMOS

Si CMOS scaling seriously stressed

→ Moore’s law threatened
The III-V view
The III-V view

The Si view
CMOS scaling in the 21st century

Si CMOS has entered era of “power-constrained scaling”:
- Microprocessor power density saturated at ~100 W/cm²

Future scaling demands $V_{DD}$↓
How to enable further $V_{DD}$ reduction?

- Transistor is switch:
  - $I_{ON}$
  - $I_{OFF}$

- Goals of scaling:
  - reduce transistor footprint
  - reduce $V_{DD}$
  - extract maximum $I_{ON}$ for given $I_{OFF}$

- The path forward:
  - increase electron velocity $\rightarrow$ $I_{ON}$ increases
  - tighten electron confinement $\rightarrow$ $S$ decreases

\[ \Rightarrow \text{use InGaAs!} \]
$L_g = 30$ nm InGaAs HEMT - Subthreshold characteristics

- $S = 74$ mV/dec
- Sharp subthreshold behavior due to tight electron confinement in quantum well
\( L_g = 30 \) nm InGaAs HEMT - Subthreshold characteristics

- \( S = 74 \) mV/dec
- At \( I_{OFF} = 100 \) nA/\( \mu \)m and \( V_{DD} = 0.5 \) V, \( I_{ON} = 0.52 \) mA/\( \mu \)m
InGaAs HEMTs: Benchmarking with Si

FOM that integrates short-channel effects and transport:
$I_{ON} @ I_{OFF}=100 \text{nA/µm}, V_{DD}=0.5 \text{ V}$

InGaAs HEMTs: higher $I_{ON}$ for same $I_{OFF}$ than Si
III-V MOSFET: possible designs

- Recessed S/D QW-MOSFET
- Regrown S/D QW-MOSFET
- Trigate MOSFET
- Nanowire MOSFET
Self-Aligned InGaAs QW-MOSFETs (MIT)

- Scaled barrier (InP: 1 nm + HfO\textsubscript{2}: 2 nm)
- 10 nm thick channel with InAs core
- Tight S/D spacing ($L_{\text{side}} \sim 30$ nm)
- Process designed to be compatible with Si fab

Lin, IEDM 2012
At $V_{DS} = 0.5$ V:
- $g_m = 1.4$ mS/µm
- $S = 114$ mV/dec
- $R_{ON} = 470 \, \Omega \cdot \mu m$
Scaling and benchmarking

- Superior behavior to any planar III-V MOSFET to date
- Matches performance of Intel’s InGaAs Trigate MOSFETs [Radosavljevic, IEDM 2011]
Long-channel InGaAs MOSFET

Barrier: InP (1 nm) + Al₂O₃ (0.4 nm) + HfO₂ (2 nm)

- $S = 69 \text{ mV/dec at } V_{DS} = 50 \text{ mV}$
- Close to lowest $S$ reported in any III-V MOSFET: 66 mV/dec [Radosavljevic, IEDM 2011]
Regrown source/drain InGaAs QW-MOSFET on Si (HKUST)

- MOCVD epi growth on Si wafer
- $n^+$-InGaAs raised source/drain
- Self-aligned to gate
- Composite barrier: InAlAs (10 nm) + $\text{Al}_2\text{O}_3$ (4.6 nm)

Zhou, IEDM 2012
Characteristics of L_g=30 nm MOSFET

At V_{DS}=0.5 V:
- \( g_m = 1.7 \text{ mS/µm} \)
- \( S = 186 \text{ mV/dec} \)
- \( R_{ON} = 157 \Omega .\mu \text{m} \)

Zhou, IEDM 2012
Multiple-gate MOSFETs

# gates ↑ → improved electrostatics → enhanced scalability

Chen, ICSICT 2008
InGaAs Trigate MOSFET (Intel)

Improved subthreshold swing as fin is made thinner

\( H_{\text{FIN}} = 40 \text{ nm} \)

Radosavljevic, IEDM 2011
InGaAs Nanowire MOSFET (Purdue)

Gu, IEDM 2011
Gu, APL 2011
Gu, EDL 2012

- $I_{on} = 720 \, \mu A/\mu m$ (86 $\mu A/wire$)
- $g_m = 0.51 \, mS/\mu m$ (61 $\mu S/wire$)
- $S = 150 \, mV/dec$

30x30 nm fin
$L_{ch} = 50 \, nm$
Barrier: 10 nm $Al_2O_3$
# wires = 4
Conclusions: exciting future for InGaAs

• Most promising material for ultra-high frequency and ultra-high speed applications
  → first THz transistor?

• Most promising material for n-MOSFET in a post-Si CMOS logic technology
  → first sub-10 nm CMOS logic?

• InGaAs + Si integration:
  → THz + CMOS + optics integrated systems?