InGaAs MOSFETs for CMOS:
Recent Advances in Process Technology

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InGaAs
High Electron Mobility Transistors

Main attractions of InGaAs:
• \( \mu_e = 6,000 - 30,000 \text{ cm}^2/\text{V.s} @ 300K \)
• \( v_{\text{inj}} = 2.5 - 3.7 \times 10^7 \text{ cm/s} @ 300 \text{ K} \)
Extraordinary recent progress of InGaAs MOSFETs

InGaAs MOSFETs

\[ g_m = 2.7 \text{ mS/\mu m} \]
Lin, IEDM 2013

*inversion-mode

Extraordinary recent progress of InGaAs MOSFETs
Technology issue #1: MOS gate stack

Challenge: metal/high-K oxide gate stack

- Fabricated through ex-situ process
- Very thin barrier (EOT ~ 0.5 nm)
- Low gate leakage ($I_G < 1$ A/cm$^2$ at $V_{GS}=0.5$ V)
- Low $D_{it}$ (<$3 \times 10^{12}$ eV$^{-1}$.cm$^{-2}$ in top ~0.3 eV of bandgap and inside CB)
- Reliable
Interface quality: 
$\text{Al}_2\text{O}_3/\text{InGaAs}$ vs. $\text{Al}_2\text{O}_3/\text{Si}$

$\text{Al}_2\text{O}_3/\text{Si}$

$\text{Al}_2\text{O}_3/\text{InGaAs}$

Close to $E_c$, $\text{Al}_2\text{O}_3/\text{InGaAs}$ comparable $D_{it}$ to $\text{Al}_2\text{O}_3/\text{Si}$ interface
Buried-channel vs. surface channel?

Classic trade-off:

- Surface channel: high scalability but low mobility ($\mu_e < 2,000 \text{ cm}^2/\text{V.s}$)
- Buried channel: high mobility but high EOT and $t_{\text{barr}} \downarrow \rightarrow \mu_e \downarrow$

InP good choice for barrier:

$\rightarrow$ wide $E_g$, lattice matched to $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$

Urabe, ME 2011
HfO$_2$ vs. Al$_2$O$_3$ in buried-channel MOSFETs

HfO$_2$ (2 nm) directly on InP (1 nm):
- Low $D_{it}$ close to $E_c$
- Steep subthreshold swing
- Low $I_{off}$ (nA/μm range)

Galatage - UT Dallas, 2012

Lin, IEDM 2012
HfO$_2$ in surface-channel MOSFETs

HfO$_2$ (2.5 nm) directly on InGaAs:
- Comparable S as buried-channel device
- EOT ↓ $\rightarrow$ $I_d$ ↑
- Low ALD temperature key

Lin, IEDM 2013

Suzuki, JAP 2012
Pristine interface for high MOS quality

- **Barrier:** InP (1 nm) + Al₂O₃ (0.4 nm) + HfO₂ (2 nm)
- **S =** 69 mV/dec at V_DS = 50 mV
- Close to lowest S reported in any III-V MOSFET: 66 mV/dec
  [Radosavljevic, IEDM 2011]

Lin, IEDM 2012
Technology issue #2: ohmic contacts

Challenge: nanometer-scale ohmic contacts with low $R_c$

- Tiny ($L_c < 30$ nm)
- Low contact resistance ($R_c < 50$ $\Omega.\mu m$)
- Self-aligned to gate ($L_{side} < 10$ nm)

![Diagram of ohmic contacts]
New “nano-TLM” test structure to characterize short contacts

Decouples impact of metal resistance on short contacts

\[
R_{\parallel} = \frac{R_{TLM}}{L_{Tx}} \text{csch} \left( \frac{W}{L_{Tx}} \right)
\]

\[
R_x = \frac{R_{TLM}}{2L_{Tx}} \left[ \text{csch} \left( \frac{W}{L_{Tx}} \right) + \text{coth} \left( \frac{W}{L_{Tx}} \right) \right] - \frac{R_{shm} W}{2L_c}
\]

Lu, EDL (submitted)
Contact-first process for Mo-InGaAs ohmic contacts

Achieved contacts with length down to 19 nm
Contact-first process preserves high-quality interface
Nanometer-scale Mo-InGaAs contacts

Mo on n⁺-In₀.₅₃Ga₀.₄₇As:

- \( R_c \) blows up for very small contacts with \( L_c < L_t = 113 \text{ nm} \)
- \( R_c \sim 40 \Omega \mu \text{m} \) for \( L_c \sim 20 \text{ nm} \)
- Average \( \rho_c = 0.69 \Omega \mu \text{m}^2 \)
- Contacts thermally stable up to 400°C

\[ L_T = 113 \text{ nm} \]
\[ 6.6 \Omega \mu \text{m} \]

Dormaier JVSTB 2012
Singisetti APL 2008
Baraskar JAP 2013
Crook APL 2007
Lin JAP 2013
Ni-InGaAs ohmic contact

- Ni diffused into InGaAs at 250°C
- Ni-InGaAs formed
- Unreacted Ni removed using HCl-based selective etchant
- $R_c \sim 50 \Omega \mu m$ demonstrated [Kim VLSI Tech 2013]

Subramanian, JES 2012

Oxland, EDL 2012

Kim, IEDM 2010
Technology issue #3: self-aligned MOSFET architectures

Challenge: ohmic contacts very closely spaced from gate
- Design of access region
- Must maintain high-quality MOS interface and low $R_c$

Gate-first process: “silicided” S/D
- Hill, IEDM 2010
- Kim, VLSI Tech 2013

Gate-first process: regrown S/D
- Egard, IEDM 2011
- Zhou, IEDM 2012
- Lee, VLSI Tech 2013

Gate-last process: recessed S/D
- Radosavljevic, IEDM 2009
- Lin, IEDM 2012
Gate-last self-aligned InGaAs MOSFETs

- Ohmic contact first (Mo)
- Extensive RIE (F-based)
- Interface exposed immediately before gate stack formation
- Process designed to be compatible with Si fab
- RIE damage annealed at 340°C:

Lin, IEDM 2012
Gate-last self-aligned InGaAs MOSFETs

- Buried-channel (EOT~0.8 nm)
- Wet semiconductor etch
- $L_{\text{side}} \sim 30$ nm

- Surface-channel (EOT~0.5 nm)
- Dry semiconductor etch + digital etch of cap
- $L_{\text{side}} \sim 5$ nm
Impact of $L_{\text{side}}$

- $L_{\text{side}} = 5 \text{ nm}, \ 2.7 \text{ mS/}\mu\text{m}$
- $L_{\text{side}} = 70 \text{ nm}, \ 1.9 \text{ mS/}\mu\text{m}$
- $L_g = 70 \text{ nm}$
- $V_{ds} = 0.5 \text{ V}$

$V_{gs}$ (V)

$g_m$ (mS/\mu m)

$L_{\text{side}} \downarrow$

$\rightarrow g_m \uparrow$

$\rightarrow S \uparrow$

$\rightarrow I_{on} \text{ at fixed } I_{off} \downarrow$

$\rightarrow \text{GIDL} \uparrow$

Lin, IEDM 2013
Technology issue #4: Tri-gate MOSFET

Challenge: acceptable $I_{ON}$ and SCE on a small-footprint
- Planar design does not provide enough “electrostatic integrity”
- Need tighter channel control through 3D device design

Planar MOSFET

Tri-gate MOSFET

Wu, IEDM 2009
Radosavljevic, IEDM 2010
Chin, EDL 2011
Radosavljevic, IEDM 2011
**Fin formation**

**Direct fin growth by Aspect Ratio Trapping**

- Some defects reach surface
- Inter-diffusion of dopant species

Fiorenza, ECST 2010
Waldron, ECST 2012

**Fin etch by RIE + digital etch**

- $\text{BCl}_3/\text{SiCl}_4/\text{Ar}$ RIE chemistry
- Digital etch: self-limiting (2 nm/cycle)
- No notching in heterostructures

Zhao, IEDM 2013
Mo contacts to fin

- Mo-first process
- Mo used as mask for fin etch

Mo sidewall contacts

- With top Mo contact:
  - $R_c \sim 7 \, \Omega \cdot \mu m$
- With sidewall contact:
  - $R_c \sim 12 \, \Omega \cdot \mu m$
Fin sidewall MOS

Double-gate sidewall MOSFET to study sidewall MOS quality

\[ \text{Mo} \quad \text{SiO}_2 \quad \text{Al}_2\text{O}_3 \quad 25 \text{ nm} \]

At sidewall:
\[ D_{it} \sim 1.4 \times 10^{13} \text{ eV}^{-1} \text{ cm}^{-2} \]
Conclusions

• Remarkable recent progress in InGaAs MOSFETs
  – $g_m$ (MOSFET) = $g_m$ (HEMT)
  – $R_{on}$ (MOSFET) < $R_{on}$ (HEMT)

• Many issues to investigate:
  – Tri-gate technology, integration with p-MOSFETs on Si, reliability