A New Self-aligned Quantum-Well MOSFET Architecture Fabricated by a Scalable Tight-Pitch Process

Jianqiang Lin, Xin Zhao, Tao Yu, Dimitri A. Antoniadis, and Jesús A. del Alamo

Microsystems Technology Laboratories, MIT
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Motivation

• Superior electron transport properties in InAs channel

[J. del Alamo, Nature 2011]
InGaAs MOSFET evolution

Performance

(Kim, IEDM 2012)

[del Alamo, ESSDERC 2013]

Fabrication and Scaling

2000s – – – – 2012

2008 (Lin) 2009 (Radosavljevic) 2010 (Radosavljevic) 2012 (Lin)
InGaAs MOSFET evolution

Performance

Kim, IEDM 2012

del Alamo, ESSDERC 2013

Fabrication and Scaling

2000s 2013

60 nm 40 nm 95 nm TaN p-InGaAs

100 nm Gate (TiN/Pt/Au)

50 nm InGaAs QW/in

InAlAs bottom barrier

50 nm SiO2 Mo (S/D) Cap Channel Buffer Mo (G)

30 nm Mo n+ Cap etch stop InGaAs/InAs/InP Buffer MoHCO3

2008 (Lin) 2009 (Radosavljevic) 2010 (Radosavljevic) 2012 (Lin) 2013 (This work)
New InGaAs MOSFET with self-aligned LEDGE

• Bottleneck to ON current is $R_{sd}$

• Introduction of highly conductive “LEDGE”
  – $n^+$ region linking metal contact and channel
Process integration

Key features: Wet-etch free / Lift-off free / Au free

Ohmic/Oxide deposition*

- SiO₂
- W/Mo
- n+ Cap
- InGaAs
- InAs
- InGaAs
- Si
- InAlAs

Gate opening

3-step gate recess

ALD deposition

HfO₂

Gate metal

Mo

Pad formation

Pad
Composite W/Mo contact

- Without W: Long undercut of Mo due to oxidation
  - Limits S/D metal spacing
- With W: No Mo oxidation

[Lin, IEDM 2012] This work
3-step gate recess process

- **CF$_4$+O$_2$ RIE**: 
  - Process enables precise control of: $t_{ch}$ / $L_{ledge}$ / $t_{ledge}$
  - Example: SiO$_2$ / W/Mo / n+ Cap

- **Cl-based RIE**: 
  - O$_2$ plasma + H$_2$SO$_4$

- **Digital etch**: 
  - O$_2$ plasma + H$_2$SO$_4$

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*Waldron, IEDM 2007*

*[Lin, EDL submitted]*
Semiconductor surface after recess

Only wet cleaning (no etching)

RMS = 0.12 nm

Scanning area: 2x2 μm²

Additional cap dry etch (~ 20 nm) + 4 cycle digital etch

RMS = 0.21 nm
Structure design: Ledge

Short Ledge

Long Ledge

$L_g=50$ nm

$L_g=70$ nm
Structure design: Ledge

Short Ledge

Long Ledge

- Surface channel: $\text{In}_{0.7}\text{Ga}_{0.3}\text{As} / \text{InAs} / \text{In}_{0.7}\text{Ga}_{0.3}\text{As} = 1/2/5$ nm
- High-k: HfO$_2$, thickness $=2.5$ nm (EOT~0.5 nm)
Output and $g_m$ characteristics for $L_g = 70$ nm

- $R_{on} = 220 \, \Omega \cdot \mu m$ for $L_{\text{ledge}} = 5$ nm
- Record $g_{m,\text{max}} = 2.7 \, mS/\mu m$ at $V_{ds} = 0.5 \, V$ for $L_{\text{ledge}} = 5$ nm
Subthreshold characteristics

- \( I_g < 10 \text{ pA/\mu m} \) over entire voltage range
  - Further EOT scaling possible

\( L_{\text{ledge}} = 70 \text{ nm} \)

\[ V_{ds} = 0.05 \text{ V} \]
\[ S_{min} = 90 \text{ mV/dec} \]
\[ DIBL = 130 \text{ mV/V} \]

\[ V_{ds} = 0.5 \text{ V} \]
\[ S_{min} = 94 \text{ mV/dec} \]

\( L_{\text{ledge}} = 5 \text{ nm} \)

\[ V_{ds} = 0.05 \text{ V} \]
\[ S_{min} = 108 \text{ mV/dec} \]
\[ DIBL = 249 \text{ mV/V} \]

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- Flattening tail at high $V_{ds}$
L_g = 20 nm InAs QW-MOSFET with L_ledge = 5 nm

- Smallest functional III-V MOSFET with tight contact spacing
Parasitic resistance analysis

For short ledge devices, major $R_{sd}$ contribution from $R_{cont}$ and $R_{bar}$
Benchmark: $I_{\text{on}}$

- Record $I_{\text{on}} = 410 \, \mu A/\mu m$ at $L_g = 70 \, \text{nm}$ for $L_{\text{edge}} = 70 \, \text{nm}$

* [Kim and del Alamo, T-ED 2008]
Short ledge MOSFETs show record $g_{m,max}$

Long ledge MOSFETs match record $S$

[Radosavljevic, IEDM 2011]
Impact of ledge on off-state leakage (Long MOSFETs)

$L_g = 200$ nm, $L_{\text{ledge}} = 70$ nm

$L_g = 500$ nm, $L_{\text{ledge}} = 5$ nm

- Short ledge leads to high $I_{\text{off}}$
- Strong $V_{ds}$ dependence

Flattening tail at high $V_{ds}$
Off-state leakage: Temperature dependence

$L_g = 500$ nm, $L_{ledge} = 5$ nm

- GIDL (gate-induced drain leakage) signature

- $I_d$ or $I_g$ (A/µm)

- $V_{gs}$ (V)

- $V_{ds}$ = 0.1 to 0.6 V

- $300K$, $150K$, $77K$
Off-state leakage follows BTBT signature

\[ J_{BTBT} \sim \exp(-A \frac{\sqrt{E_g}}{V_{dg}}) \]

- \( I_s \) follows BTBT dependence on \( V_{dg} \) and \( E_g \)

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TCAD simulation of BTBT rate based on nonlocal path BTBT model:
Conclusions

• Novel self-aligned III-V QW-MOSFETs:
  – Lift-off free, wet-etch free, and Au free in front end process
  – Design and fabrication of critical S/D ledge
  – Tight metal contact spacing
  – Scaled channel thickness, barrier thickness and gate length

• Record results demonstrated:
  – \( g_{m,\text{max}} = 2.7 \, \text{mS/}\mu\text{m} \) in \( L_{\text{ledge}} = 5 \, \text{nm} \)
  – \( I_{\text{on}} = 410 \, \mu\text{A/}\mu\text{m} \) in \( L_{\text{ledge}} = 70 \, \text{nm} \)

• Characteristic GIDL signature observed