Vertical Nanowire InGaAs MOSFETs
Fabricated by a Top-down Approach

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Outline

• Motivation

• Device technology

• Device electrical characteristics

• Conclusions
Motivation

Superior electron transport properties of InGaAs material system – high mobility and electron velocity

del Alamo, Nature 2011
Gate-all-around (GAA) nanowire MOSFETs

- Nanowire MOSFET provides ultimate scalability

Kuhn, TED 2012
Vertical channel MOSFETs

Vertical nanowire decouples footprint scaling and gate length scaling → high density

• Use of vertical FETs saves 40% of total chip area

Liu, DRC 2012
Impressive devices via bottom-up techniques demonstrated

- Complicated epitaxial growth or Au seed particles required

- Top-down approach worth investigating!
Goal: vertical nanowire InGaAs MOSFETs fabricated via top-down approach

Starting heterostructure:

- n+ InGaAs, 70 nm
- i InGaAs, 80 nm
- n+ InGaAs, 300 nm

n+: $6 \times 10^{19}$ Si doping

Key elements:

- Top-down approach based on RIE
- Single nanowire MOSFETs
Process flow

Starting substrate

InGaAs

n+

i

n+

Adhesion layer

HSQ

n+

i

n+

Sputtered W

ALD-Al₂O₃

1st SOG

Mo/Ti/Au

2nd SOG

Tomioka, Nature 2012
Persson, DRC 2012
Key enabling technology: RIE by BCl$_3$/SiCl$_4$/Ar Chemistry

- Sub-20 nm resolution
- Aspect ratio > 10
- Smooth sidewall and surface
- BCl$_3$/SiCl$_4$/Ar RIE chemistry used for III-V optical devices, never used for nm-scale features
Critical parameter:
Substrate temperature during RIE

$T \uparrow \Rightarrow \text{etch rate} \uparrow$, surface roughness $\downarrow$, sidewall verticality $\uparrow$
Nanowire RIE followed by \textit{digital etch}

Digital etch:
- self-limiting $O_2$ plasma oxidation + $H_2SO_4$ oxide removal

Lin, IEDM 2012

before after 10 cycles

- Shrinks NW diameter by 2 nm per cycle
- Unchanged shape
- Reduced roughness
Planarization and etch back

After 1\textsuperscript{st} planarization

After 2\textsuperscript{nd} planarization
NW-MOSFET I-V characteristics
D= 30 nm

Single nanowire MOSFET:
- D= 30 nm
- L<sub>ch</sub>= 80 nm
- 4.5 nm Al<sub>2</sub>O<sub>3</sub> (EOT = 2.2 nm)

At V<sub>Ds</sub>=0.5 V (normalized by periphery):
- g<sub>m, pk</sub>=280 μS/μm
- R<sub>on</sub>=759 Ω.μm

V<sub>gs</sub>=-0.6 V to 0.8 V in 0.1 V step
R<sub>on</sub>=759 Ω.μm (at V<sub>gs</sub>=1 V)
D=30 nm InGaAs NW-MOSFETs

$$V_{ds} = 0.5 \text{ V}$$

$$I_d < 10^{-9} \text{ A/µm}$$

$$V_{ds} = 0.05 \text{ V}$$

DIBL = 195 mV/V

S = 145 mV/dec, $$V_{ds} = 0.05 \text{ V}$$

S = 200 mV/dec, $$V_{ds} = 0.5 \text{ V}$$
D=50 nm InGaAs NW-MOSFET

At $V_{ds}=0.5$ V:
- $g_{m, pk}=730 \mu S/\mu m$
- $R_{on}=310 \Omega.\mu m$
D=50 nm InGaAs NW-MOSFETs

\[ V_{ds} = 0.5 \text{ V} \]

\[ I_g < 10^{-10} \text{ A/\mu m} \]

\[ V_{ds} = 0.05 \text{ V} \]

DIBL=360 mV/V
S=210 mV/dec, \( V_{ds} = 0.05 \text{ V} \)
S=305 mV/dec, \( V_{ds} = 0.5 \text{ V} \)
Impact of nanowire diameter

- $V_{ds} = 0.5$ V
- $V_{ds} = 0.05$ V

$S$ (mV/dec)

Error bars indicate distribution of ~10 devices

$D$ ↓ → $S$ ↓, DIBL ↓, $g_m$ ↓, $R_{on}$ ↑
Impact of digital etch

Single nanowire MOSFET:
- $D = 40$ nm (final diameter)

Digital etch $\rightarrow$ $S \downarrow$, $g_m \uparrow$, $I_g \downarrow$
- Better sidewall interface
- $R_{on}$ and DIBL unchanged

\[ V_{gs}(V) \]
\[ I_d \text{ (A/µm)} \]
\[ V_{ds}=0.5 \text{ V} \]
\[ V_{ds}=0.05 \text{ V} \]

\[ V_{gs}(V) \]
\[ V_{ds}=0.5 \text{ V} \]

\[ V_{gs}(V) \]
\[ I_g \text{ (A/cm}^2) \]
\[ V_{ds}=1 \text{ V} \]
Benchmarking against bottom-up vertical InGaAs NW-MOSFETs

- Fundamental trade-off between transport and short-channel effects
- Top-down NW-MOSFETs as good as bottom up devices
Conclusions

• First demonstration of top-down III-V GAA NW-MOSFET with vertical channel
  • Novel III-V RIE process with sub-20 nm resolution
  • 30 nm diameter NW MOSFET achieved

• Digital etch improves subthreshold and transport characteristics

• Device performance matches that of best bottom-up vertical NW III-V MOSFETs
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