Anomalous Source-side Degradation of InAlN/GaN HEMTs under ON-state Stress

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Outline

1. Motivation
2. Source-side degradation under ON-stress
3. Gate leakage current and its temperature dependence
4. Positive gate stress
5. Conclusions
Motivation: InAlN as barrier

- High spontaneous polarization in InAlN $\rightarrow$ high 2DEG density
- InAlN thickness scaling $\rightarrow$ gate length scaling $\rightarrow$ W- and V-band applications

<table>
<thead>
<tr>
<th></th>
<th>$\text{Al}<em>{0.2}\text{Ga}</em>{0.8}\text{N}/\text{GaN}$</th>
<th>$\text{In}<em>{0.17}\text{Al}</em>{0.83}\text{N}/\text{GaN}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta P_0$ (e$\cdot$cm$^{-2}$)</td>
<td>$6.5 \times 10^{12}$</td>
<td>$2.7 \times 10^{13}$</td>
</tr>
<tr>
<td>$P_{\text{piezo}}$ (e$\cdot$cm$^{-2}$)</td>
<td>$5.3 \times 10^{12}$</td>
<td>$0$</td>
</tr>
<tr>
<td>$P_{\text{total}}$ (e$\cdot$cm$^{-2}$)</td>
<td>$1.2 \times 10^{13}$</td>
<td>$2.7 \times 10^{13}$</td>
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[J. Kuzmik, EDL 2001]

$\text{In}_{0.17}\text{Al}_{0.83}\text{N}$ lattice matched to GaN $\rightarrow$ Potentially better reliability!
Motivation: InAlN as barrier

InAlN/GaN HEMTs
• W-band
• E-mode

Four gate geometries:
• $W_g = 8 \times 25 \, \mu m$
• $W_g = 8 \times 50 \, \mu m$
• $W_g = 2 \times 25 \, \mu m$
• $W_g = 2 \times 50 \, \mu m$

Thermal models available

[Saunier, CSICS 2014]
High-$V_{DS}$-high-$I_D$ stress

Stress and characterization conditions:

- $V_{DS,\text{stress}} = 25\ \text{V}$, $I_{D,\text{stress}} = 400\ \text{mA/mm}$ ($V_G \sim 1.5\ \text{V}$), 5 mins, RT ($T_j \sim 136\ \text{°C}$)
- Characterization: @ 25 °C after thermal detrapping

![Graph showing $I_D$ vs $V_{DS}$ with $V_G = 2\ \text{V}$](image)

![Graph showing $I_D$ vs $V_{GS}$ with $V_{DS} = 0.1\ \text{V}$](image)

Permanent degradation:  
- Significant $I_{D,\text{max}}$ degradation  
- $\Delta V_T > 0$  
- Significant $I_{D,\text{off}}$ degradation
High-$V_D$-high-$I_D$ stress

After thermal detrapping, gate current degradation:

- Large increase in $I_G$ after stress
- After stress: $I_G = I_S >> I_D$ in forward and reverse bias
- Source-side damage unexpected!
- Uncommon but previously observed in AlGaN/GaN HEMTs [J. Joh, IEDM 2010]
Temperature dependence of $I_G$ and $I_D$

**Before stress:**
- For moderate $V_{GS}$, negative T coefficient $\rightarrow$ thermionic emission limited current
- $I_S$ behaves similar to $I_G$

**After stress:**
- Significantly reduced T dependence for $I_G$ and $I_S$
- $I_D$ less affected $\rightarrow$ degradation on source side
HRTEM of a virgin device

Virgin device
drain side

Virgin device
source side

Passivation

InAlN

GaN

AlN

Gate metal

Residual oxide?

Gate recessed to the AlN interlayer
HRTEM of stressed device

Disordered region in GaN channel at gate edge on source side
Hypothesis for Damage

High $V_{DS,\text{stress}}$ + high $I_{D\text{stress}} \rightarrow$ high $I_{G\text{stress}}$ too

$\rightarrow$ high $I_{GS}$

$\rightarrow$ high $T_j$

$\rightarrow$ high electric field across AlN barrier on source side

Conditions favor defect formation in AlN barrier on source side $\rightarrow I_{GS} \uparrow$

Also, gate sinking $\rightarrow \Delta V_T > 0$
Positive $V_G$ step-stress-recovery experiment

Stress and characterization conditions:

- $V_{GS,\text{stress}} = 0 - 2.5$ V, $V_{DS,\text{stress}} = 0$ V, step = 0.1 V, RT ($T_j \sim 48$ °C)
- Characterization: @ 25 °C after thermal detrapping

**Permanent degradation:**

- Significant $I_{D_{\text{max}}}$ degradation
- $\Delta V_T > 0$
- Significant $I_{D_{\text{off}}}$ degradation
Time evolution of $I_{D\text{max}}$ and $I_{G\text{off}}$

Stress conditions:
- $V_{DS,\text{stress}} = 0$ V, $V_{GS,\text{stress}} = 0.1 – 2.5$ V in 0.1 V steps
- stress time = recovery time = 150 s; characterization every 15 s
- RT

![Graph showing $I_{G\text{off}}$ as a function of time and stress voltage](image)

- $|I_{G\text{off}}|$ starts to increase from $V_{GS,\text{stress}} \approx 1.7$ V $\rightarrow$ trap generation in AlN
- $I_{D\text{max}}$ starts to severely degrade from $V_{GS,\text{stress}} \approx 2.3$ V $\rightarrow$ gate sinking
Time evolution of $I_{G\text{stress}}$

Stress conditions:

- $V_{DS,\text{stress}} = 0$ V, $V_{GS,\text{stress}} = 0.1 – 2.5$ V in 0.1 V steps
- stress time = recovery time = 150 s; characterization every 15 s
- RT

\begin{itemize}
  \item $I_{G\text{stress}}$ increase becomes significant for $V_{GS,\text{stress}} \geq 2.3$ V
\end{itemize}
Gate current degradation

After thermal detrapping, gate current degradation:

- Symmetric degradation: $I_S \approx I_D \approx I_G/2$
- Reproduced degradation signature of high-$V_{DS}$-high-$I_D$ stress: high forward $V_G$ leads to increase in $I_G$
HRTEM of stressed device

Disordered region in GaN channel at gate edge on drain side

Disordered region in GaN channel at gate edge on source side
Conclusions

• Permanent degradation after High-$V_{DS}$-high-$I_D$ stress:
  - $I_{Goff} \uparrow\uparrow \rightarrow$ Defect formation in AlN barrier on source side
  - $\Delta V_T > 0$, $I_{Dmax} \downarrow\downarrow \rightarrow$ Gate sinking
  - Affects source side

• Positive gate stress:
  - Reproduced degradation signature of high-$V_{DS}$-high-$I_D$ stress:
    - $I_{Goff} \uparrow\uparrow$, $\Delta V_T > 0$, $I_{Dmax} \downarrow\downarrow$
    - $I_S \sim I_D \sim I_G/2 \rightarrow$ Symmetric degradation on source and drain side
Thank you & Questions?