Electric-Field Induced F⁻ Migration in Self-Aligned InGaAs MOSFETs and Mitigation

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Outline

• Background: F in III-V’s
• F-Induced Instability in InGaAs MOSFETs
• Independent confirmation of F role
• Mitigation
• Conclusions
F-Induced Donor Passivation

- F known to migrate to Si:InAlAs, and passivate Si donors


F-Si complex observed


Electron concentration

Selective F passivation

- F only affects n-InAlAs, but not InP or InGaAs

- InAlAs has strong tendency of ionization
- AlAs:InAs=1:1 gives the most localization of F due to ionic radius difference between Al and In

F-Induced Instability

• F-donor complex weakly bound

![Graph showing carrier concentration vs. re-annealing time. T=400 °C, UHV.](image1)

N. Hayafuji et al, APL 1995

![Diagram illustrating thermal annealing and electric field.](image2)

N. Hayafuji et al, APL 1996

• Under high temperature or electric field, F\(^-\) bound to Si in InAlAs can easily dissociate and migrate
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Self-aligned InGaAs MOSFETs

- Gate dielectric: 2.5 nm HfO₂
- Intrinsic channel: In₀.⁷Ga₀.₃As/InAs/In₀.⁷Ga₀.₃As (1/2/5 nm)
- Composite n⁺ cap: n-InGaAs/n-InP/n-InAlAs/i-InP
- Access region length: 85 nm
F in self-aligned InGaAs MOSFETs

- Si:InAlAs used in cap and access regions
- Process involves F-based RIE + thermal annealing

- F expected to concentrate under gate and in access regions
- Consequences:
  - $n_s \downarrow$, $R_{on} \uparrow$, $g_m \downarrow$ in virgin device
  - Reduced current drive
  - Device instability due to F migration

J. Lin et al, IEDM 2013
During stress, F⁻ drifts from access regions into gate oxide, reactivating Si dopants in n-InAlAs in access region

- \( n_s \uparrow \), \( R_{on} \downarrow \) and \( g_m \uparrow \)

During recovery, F⁻ diffuses back to n-InAlAs and passivates Si donors

- \( n_s \downarrow \), \( R_{on} \uparrow \) and \( g_m \downarrow \) revert to virgin state: complete recovery
Forward Gate Stress

- Comparison with Positive Bias Temperature Instability (PBTI) study in other InGaAs MOSFETs:

  This work: $g_m \uparrow$ vs. PBTI: $g_m \downarrow$
  This work: fast vs. PBTI: slow
Forward Gate Stress

- Positive gate voltage stress at different $V_{gt, stress}$

- $\Delta g_{m,max} - \Delta V_{t,lin}$ correlation inconsistent with established PBTI

- No universal relation between $\Delta g_{max}$ and $\Delta V_{t,lin}$
Forward Gate Stress

- Positive gate voltage stress at different $V_{gt, stress}$

- Universal relation between $\Delta g_{max}$ and $\Delta R_{on}$

- Connection between $g_m$ instability and extrinsic portion of the device
Off-State Stress

- Stress: $V_{gt}=0 \text{ V}$, $V_{ds}=0.7 \text{ V}$, 2 h, at RT

- Lateral E-field sweeps $F^-$ away from source and gate oxide towards drain
  - On source side: Si dopants reactivated, $g_m$ ↑ in forward mode
  - On drain side: Si dopants passivated, $g_m$ ↓ in reversed mode

![Graph showing $g_m$ vs $V_{gs}$ for forward and reversed S/D modes, with stress conditions and channel diagram indicating off-state voltage stress ($V_{ds}>0 \text{ V}$).]
Temperature Dependence

• Forward gate stress: $V_{gt} = 0.8$ V, $V_{ds} = 0$ V, 2 h, at various $T$

• Recovery: $V_{gs} = 0$ V, $V_{ds} = 0$ V, 1.5 h, at same stress $T$

$E_A = 0.23 \pm 0.05$ eV, consistent with estimated F-Si ionization energy (A. Taguchi et al, Phys. Rev. B 2000)
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Independent Confirmation: SIMS

- 3 samples containing 3 nm-thick buried Si:InAlAs layer

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>never exposed to F</td>
</tr>
<tr>
<td>B</td>
<td>exposed to Mo sputtering and F-based RIE</td>
</tr>
<tr>
<td>C</td>
<td>Process of B + annealing at 350°C &amp; 1 min</td>
</tr>
</tbody>
</table>

- Samples B and C show high surface concentration of F
- Sample C shows additional pile-up in Si:InAlAs layer
- Verifies F migration to Si:InAlAs in our structure
Independent Confirmation: TLM

- Sample with cap containing 3 nm-thick Si:InAlAs
- TLMs measured before and after annealing at 350°C for 1 min

<table>
<thead>
<tr>
<th>Sample #</th>
<th>Mo Contact Process</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>lift-off (no exposure to F)</td>
</tr>
<tr>
<td>B</td>
<td>sputtered and etched by SF$_6$/O$_2$ RIE</td>
</tr>
<tr>
<td></td>
<td>(as in MOSFET process)</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>Lift-off (F-free)</th>
<th>F-RIE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>before annealing</td>
<td>after annealing</td>
</tr>
<tr>
<td></td>
<td>before annealing</td>
<td>after annealing</td>
</tr>
</tbody>
</table>

- F-free sample: annealing $\Rightarrow R_{sh} \downarrow$
- F-RIE sample: annealing $\Rightarrow R_{sh} \uparrow$ by 3X
- Verifies F$^-$ induced donor passivation in our process
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Mitigation: New MOSFET Structure

- Potential solution: **eliminate Si:InAlAs**
- New device structure: **use n-InP in access region**

**Original device structure**

<table>
<thead>
<tr>
<th>Layer</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mo/W</td>
<td></td>
</tr>
<tr>
<td>( n^+ ) InGaAs (10 nm)</td>
<td></td>
</tr>
<tr>
<td>( n^+ ) InP (9 nm)</td>
<td></td>
</tr>
<tr>
<td>( n^+ ) InAlAs (3 nm)</td>
<td></td>
</tr>
<tr>
<td>InP (3 nm)</td>
<td></td>
</tr>
<tr>
<td>InGaAs/InAs/InGaAs (3/2/5 nm)</td>
<td></td>
</tr>
<tr>
<td>InAlAs (5 nm)</td>
<td></td>
</tr>
<tr>
<td>InAlAs (25 nm)</td>
<td></td>
</tr>
<tr>
<td>InP (6 nm)</td>
<td></td>
</tr>
<tr>
<td>InAlAs (400 nm)</td>
<td></td>
</tr>
</tbody>
</table>

**New device structure**

<table>
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<tr>
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<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mo/W</td>
<td></td>
</tr>
<tr>
<td>( n^+ ) InGaAs (10 nm)</td>
<td></td>
</tr>
<tr>
<td>( n^+ ) InP (14 nm)</td>
<td></td>
</tr>
<tr>
<td>InGaAs/InAs/InGaAs (3/2/5 nm)</td>
<td></td>
</tr>
<tr>
<td>InAlAs (25 nm)</td>
<td></td>
</tr>
<tr>
<td>InP (4 nm)</td>
<td></td>
</tr>
<tr>
<td>InAlAs (400 nm)</td>
<td></td>
</tr>
</tbody>
</table>

**Access length**

- Original: \( L_{access} = 85 \) nm
- New: \( L_{access} = 15 \) nm
Improved Electrical Stability

- Response to forward gate stress ($V_{gt}=0.8 \text{ V}$ and $V_{ds}=0 \text{ V}$)

- New device: $g_{m,max}$ ↓ (up to 15%), small $\Delta V_t >0$, classic PBTI behavior
Improved Electrical Stability

- Response to off-state stress \((V_{gt}=0 \text{ V and } V_{ds}=0.7 \text{ V})\)

- New device: minimal change

![Graphs showing comparison between Original Structure and New Structure](image-url)
Classical PBTI Behavior

- Positive gate voltage stress at different $V_{gt,\text{stress}}$ at RT

- $\Delta V_{t,\text{lin}}$ follows power law with time exponent $n \sim 0.23-0.44$

- Strong correlation between $\Delta g_{\text{max}}$ and $\Delta V_{t,\text{lin}}$ at different $V_{gt,\text{stress}}$ at RT

- Typical of PBTI
Classical PBTI Behavior

- Positive gate voltage stress at different $V_{gt,\text{stress}}$ at RT

\[ \Delta V_t \propto (V_{gs} - V_t)^\gamma \]

- Stress voltage exponent $\gamma \sim 1.3$-$1.8$, similar to other studies in InGaAs MOSFETs PBTI

N. Agrawal et al, EDL 2015
Weak Temperature Dependence

- Forward gate stress: $V_{gt} = 0.8 \, V$, $V_{ds} = 0 \, V$, 2 h, at different $T$
- New structure: reduced $V_t$ sensitivity with $T$
- Weak $T$ dependence with $E_A = 0.062 \pm 0.004$ eV
- Characteristic of border traps that communicate through tunneling

![Graph showing temperature dependence and new structure](image-url)
Record Performance

- Absence of Si:InAlAs mitigates F donor passivation $\Rightarrow R_{on} \downarrow \Rightarrow g_m \uparrow$

- $R_{on} = 190 \, \Omega \cdot \mu m$

- $g_{m,\text{max}} = 3.45 \, \text{mS/\mu m}$ (new record for InGaAs FETs of any kind)

J. Lin et al., EDL (2016)
Conclusions

• Identified instability mechanism in self-aligned InGaAs MOSFETs caused by F⁻ migration and (de)-passivation of Si dopants in InAlAs

• Successfully mitigated problem by eliminating Si:InAlAs from device structure

• New device design achieved improved stability and record device performance

Thank you!