Digitally Assisted and Hybrid Architectures for RF Transceivers in Deep-Submicron CMOS

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Outline

• Keys to meaningful digitally assisted architectures.

• Low-offset mixers, multipliers, and VGAs.

• New PA linearization technique.
A milestone in transceiver architectures

Superheterodyne receiver, Armstrong, 1917.

Astounding achievement…allows for huge gain from antenna to audio out without feedback problems.
What drives current research?

• Making the most of available spectrum.

• Communications with the lowest possible power consumption.

• Making CMOS transceivers work despite extreme scaling.
Keys to meaningful digitally assisted architectures

• Exploit the superior time-domain resolution of digital edge transitions in advanced CMOS processes. [B. Staszewski]

• Optimally partition functionality between analog and digital domains.
  – Sometimes this means digital correction of “sloppy” analog.
  – Sometimes this means a more complete co-design of analog and digital parts.
Chopper-stabilized mixers, multipliers, and VGAs

- At least two different choices for chopping waveforms:
  - Quadrature square waves at $f_0$ for chopping, square wave at $2f_0$ for down chopping
  - Orthogonal spreading codes (e.g. Gold codes) for chopping
Measured spectrum comparison: Square wave vs. Gold code chopping

- Choice of waveforms depends on application.
- Prototype IC fabricated in 0.18μm CMOS process.
How good is the offset performance?

<table>
<thead>
<tr>
<th>Inner Chopper</th>
<th>Outer Chopper</th>
<th>$V_x$</th>
<th>$V_y$</th>
<th>$V_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>15.6 mV</td>
</tr>
<tr>
<td>Square-wave @ 100kHz</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>0.36 μV</td>
</tr>
<tr>
<td>Square-wave @ 100kHz</td>
<td>-</td>
<td>0</td>
<td>150mV</td>
<td>6.06 μV</td>
</tr>
<tr>
<td>Square-wave @ 100kHz</td>
<td>-</td>
<td>150mV</td>
<td>0</td>
<td>4.00 μV</td>
</tr>
<tr>
<td>Square-wave @ 100kHz</td>
<td>Square-wave @ 10kHz</td>
<td>0</td>
<td>150mV</td>
<td>0.66 μV</td>
</tr>
<tr>
<td>Square-wave @ 100kHz</td>
<td>Square-wave @ 10kHz</td>
<td>150mV</td>
<td>0</td>
<td>1.52 μV</td>
</tr>
<tr>
<td>7-bit Gold code over 100kHz</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>123 μV</td>
</tr>
<tr>
<td>9-bit Gold code over 100kHz</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>30.6 μV</td>
</tr>
<tr>
<td>11-bit Gold code over 100kHz</td>
<td>-</td>
<td>0</td>
<td>0</td>
<td>7.8 μV</td>
</tr>
</tbody>
</table>

- With both inputs zero, output offset is **360nV**! (Limited by parasitic thermocouples).
- Use nested chopping to get 1.5μV worst-case offset.
- Orthogonal gold code spreading gives offset that goes as $1/2^n$, as expected.
Chopper stabilized multipliers as “digitally assisted”

Exploit superior time-domain resolution of digital edge transitions in advanced CMOS processes.

Chopping depends on precise, 50% duty cycles in chopping waveforms.

Optimally partition functionality between analog and digital domains.

Use two A/Ds, a digital multiplier, and a D/A? Cumbersome.

Use digital to clean up “sloppy” analog?

Not in this case! Analog and digital completely co-designed.
Problem: Need the power amplifier to be both linear \textit{and} efficient.
Linearity vs. power efficiency

Power efficiency $\iff$ Battery lifetime
Thermal management

Linearity $\iff$ Sophisticated Modulation Techniques $\iff$ Spectral efficiency
Linearization: getting the best of both worlds

- Static digital predistortion
- Feedback linearization
- Adaptive predistortion
Cartesian feedback

- Invulnerable to drift, forgiving of poor PA model.

- Group delay of SAW forces severe BW limitation.
Digital assistance:
Cartesian feedback to train a predistorter!

- Keeps modeling simple, escapes BW limit!
Digitally assisted CFB, part I

- Slowly step through all symbols, and fill LUT.
Digitally assisted CFB, part II

- Transmit using open-loop digital predistortion.
- Retrain as needed.
Overview of advantages

• Cartesian loop no longer needs to be fast
  – Allows low-power, highly accurate A/Ds
  – Relaxes the noise requirements of downconversion path
  – Permits “exotic” options for summers and loop filters (e.g., switched-capacitor techniques)
• PA modeling greatly simplified; no convergence issues
• Cartesian LUT more general than AM-AM and AM-PM
• Ideal for high-bandwidth transmission
• Robust to drift, aging, and process variations
• Exploits relative insignificance of PA memory effects in handsets
Discrete-component prototype overview

- A/D conversion provided by digital oscilloscope
- LUT and D/A conversion done via arbitrary waveform generator
- Digital filtering and test signal generation performed in MATLAB
The experimental system
Exploit slow training: reduce noise by averaging

- Excessive downconversion noise (due to oscilloscope capture) reduced by averaging several measurements.
- RMS noise voltage goes down as $N^{-1/2}$. 
Minimize training time: take few samples, and interpolate

- Introduces “interpolation noise.”
Fix interpolation noise with filtering

- Extra filter reduces high-frequency artifacts.
Check of closed-loop CFB system

- For 28dBm power output, 22dB reduction in 3\textsuperscript{rd}-order products.
  - 1dB compression point of PA is 27dBm.
Wideband predistortion: EVM measurement

- 16-QAM signals with 2MHz bandwidth.
- Output power is 28dBm.
Very wideband predistortion: 40MHz channel

- 10dB of distortion product reduction with no degradation in noise floor.
- Exceeds WiMax channel bandwidths.
Two remaining issues

• While lookup table is being filled, symbols are transmitted!
  – And what about antenna impedance variation once LUT is set?
• Can this work for OFDM, where the number of possible symbols is so high?
Fill the LUT while transmitting into dummy 50Ω load

• Takes care of transmitting during training, but what about impact of antenna impedance variations?
Training on dummy load, transmitting with VSWR of 1.4 and 2.0

- **VSWR = 1.4**
  - (S11 = -16dB)

- **VSWR = 2.0**
  - (S11 = -10dB)
Training on dummy load, transmitting with VSWR of 3.0

- Predistortion shows benefits even for VSWR of 3.0.
- In our experiments with an antenna, we never observed its VSWR to be this severe.
Use interpolation between LUT points to transmit mobile WiMAX-OFDMA signal

- Measured spectrum transmitted into a real antenna after dummy load training
- 5 MHz wide channel
- 256 LUT entries; bilinear spline interpolation.
- Training time: 2ms
The bottom line: power savings of 23%
Review of Advantages

• Cartesian loop no longer needs to be fast
  – Allows low-power, highly accurate A/Ds
  – Relaxes the noise requirements of downconversion path
  – Permits “exotic” options for summers and loop filters (e.g., switched-capacitor techniques)
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PA linearization technique as “digitally assisted”

Exploit superior time-domain resolution of digital edge transitions in advanced CMOS processes.

- Starts with a continuous time system and relies on sampling to greatly increase linearization BW.

Optimally partition functionality between analog and digital domains.

- Allow analog to do the modeling; let digital provide the speed and noise reduction.

Use digital to clean up “sloppy” analog?

- Some (averaging to reduce noise, plus digital interpolation), but analog brings elegant modeling method to the table.
Conclusion

• Digitally assisted architectures are an extremely interesting consequence of CMOS scaling.

• There are *many* ways to take advantage of digital circuits:
  – Calibration
  – Digital compensation for analog impairments
  – Clever use of CMOS switches
  – Using “digital” topologies for analog functions
  – Encoding information in timing of digital edges
  – …and more to come!