

Comparisons of Conventional, 3D, Optical and RF Interconnects for On-Chip Clock Distribution

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ABSTRACT- This paper analyses the performance of different interconnect technologies for on-chip clock distribution, including conventional, three-dimensional (3D), optical, and RF interconnects. Skew, power, and area usage were estimated for each of these technologies based on the 2001 International Technology Roadmap for Semiconductors (ITRS). Our results indicate that most of the skew and power are associated with local clock distribution. Consequently, since the alternative clock distribution approaches that have been proposed focus on global clock distribution, we have not found significant advantages over conventional clock distribution in terms of skew and power. Furthermore, it was found that low skews could be attained with conventional clock distribution schemes if the clock signals are not scaled down.

I. INTRODUCTION

The continuous scaling down of the physical dimensions of transistors, which has beneficial effects on their performance and enables a larger number of transistors per unit area, requires a growing number of interconnects. Unfortunately, since the performance of interconnects does not improve by scaling down their dimensions, they are becoming the performance limiter of high performance microprocessors (for example, see [1-3]). The 2001 International Technology Roadmap for Semiconductors (ITRS) predicts that the number of transistors integrated on a single die will exceed one billion by 2010. This growing number of transistors and the increasing clock frequencies translate into an increasing fraction of the total power being consumed in clock distribution. In addition, the budgets for skew and jitter are rapidly decreasing with increasing frequency, typically as the inverse of the frequency. As a consequence of the increasing power and decreasing budgets for skew and jitter, the design of the on-die clock distribution network is an increasingly challenging task.

Currently, a digital (and electrical) clock signal is distributed using metallic interconnects (e.g. Cu) throughout the entire die. There are many approaches to distribute digital clock signals, such as H-trees, grids and some combinations of them [4-5]. In this paper, we will consider buffered H-trees driving local grids as representative of present clock distribution, to which we will refer as conventional approach. Advanced active de-skewing techniques, which further improve the quality of standard clock distribution, are not considered in this simple analysis [5].

Several interconnect solutions have been proposed to mitigate the increasingly difficult clock distribution, 3-D, optical, and RF being the most important ones. 3-D interconnects, which refers to two or more active Si strata that are integrated together (for example by bonding), take advantage of the vertical dimension to decrease the die size, therefore alleviating clock distribution (see, for example, [6-9]). Optical interconnects have also been proposed for clock distribution since they are immune to crosstalk noise from adjacent electrical interconnects, and because of their speed-of-light propagation. Optical interconnects also have the potential for large bandwidths, which are mostly relevant for signaling [10-11]. RF approaches using Cu interconnects have been proposed as a low-power clock distribution alternative at the package level [12], but in this work we will assume that they can also be implemented on die, to explore their potential for a performance improvement. The main difference between the RF approach considered in this work and conventional approaches is that RF uses a narrow-band sinusoidal wave for transmitting the clock signal as opposed to the digital square signal that is employed in conventional clock distribution. An interesting wireless RF clock distribution, in which the clock signal is broadcasted by a source and received by on-die antennae, has also been proposed and investigated in

Ref. [13], but will not be considered in this paper. This technique is attractive since it does not require interconnects. However, noise considerations as well as the size and position of the antennae are technical and cost issues that have to be addressed.

Most of the benchmarking research has been confined to global clock distribution. However, in order to truly assess the overall benefits of alternative clock distribution approaches, it is also important to include the local clock distribution in the analysis. In this paper, simple analytical models are used to calculate clock skew, power, and area usage for conventional, 3-D, optical and RF technologies at different technology nodes, using data from the 2001 ITRS and the literature.

II. MODELS AND METHODOLOGIES

A. Conventional clock Distribution

As an example, a buffered H-tree clock distribution network with four levels ($n = 4$) is shown in Fig. 1. A useful property of H trees is that the distance between the driver and any distribution point at the end of the branches is equal (assuming the H-tree is well balanced). Buffers are typically placed at the end points of the H-tree to drive a grid and at the points where interconnects branch into two interconnects. In addition, repeaters are usually inserted along the interconnects that form the H-tree to minimize delay and mitigate the effects of dispersion. In order to compare the performance under a general and simplified situation, the H-tree is assumed to be perfectly balanced, which is not easily achieved in practice.

The conventional clock distribution can be divided into three parts: (1) H-Tree, (2) buffers, and (3) grids from which sequential elements receive the clock signal. Before proceeding further, it is important to distinguish between local and global clock distribution. In this paper, the global distribution network consists of the H-tree itself. Any components after the buffers at the end of the H-tree such as grids and the latches comprise the local distribution. Thus, the local and global distribution networks together with the buffers at the end of the H-tree, comprise the entire clock distribution network.

B. Alternative interconnect technologies

The interconnect technologies are compared using clock skew, power and area usage as metrics. Fig. 2 shows schematic diagrams of the clock distribution considered in this paper. In all cases, the total die area, A , is 1 cm^2 (in the 3D case, there are two 0.5 cm^2 die). Inductive effects and crosstalk are ignored in this analysis.

Table 1 lists the components for each interconnect technology. It is important to mention that the different approaches only differ at the global level, while the local

part of the clock distribution is identical for all cases. Therefore, all interconnect technologies exhibit the same local performance. However, for the global distribution, it is expected that performance will vary amongst different technologies.

Only two Si strata are considered for 3-D interconnects, which results in a smaller die, with an area of $0.5A$ (compared to A in the other technologies). In addition, the effects of vias between the two die is ignored. Except for these two differences, clock distribution is identical for the conventional and 3D cases. RF clock distribution is accomplished using sinusoidal waves into an H-tree, which is transformed into a digital signal by an amplifier at the end of the H-tree and then amplified. RF clocks have mostly been proposed for on-package clock distribution, and there might be technical challenges for its on-die implementation. Nevertheless, in this work we will assume that it is technically feasible. Finally, for optical clock distribution, we consider an H-Tree structure built using waveguides. At the end points of the H-tree detectors convert the light pulses into electrical currents, which are then converted into voltage pulses that are amplified to obtain a full-swing electrical clock signal.

Implementation of alternative clock distribution techniques not only requires performance advantages, but also demands overcoming additional technical challenges, such as integration with existing processes, low manufacturing cost and high yields, as well as robustness to design errors and manufacturing excursions. The lack of reliable and realistic integrated data for alternative clock distribution schemes also increases the technological risk, since unexpected problems could arise late in the development. Consequently, to motivate research and development of alternative interconnects large performance advantages are typically required. As was already mentioned, the goal of this paper is to assess the potential performance advantages under common metrics to provide insights into the driving force for developing alternative clock distribution schemes.

C. Clock Skew

Skew is defined as the time difference between the maximum and minimum delays of the rising edge of the same clock pulse at different places in the die. Although zero clock skew can be achieved in principle by designing perfectly balanced H-trees, clock skew resulting from process variations is unavoidable [14]. Therefore, even a perfectly balanced H-Tree structure has clock skew.

The local and global clock skew introduced by process variations and voltage fluctuations were calculated using the range of variation reported in the 2001 ITRS and Ref. [15].

(1) Local and Buffer Skew for All Technologies

As mentioned earlier, because it is assumed that all technologies have the same local clock distribution, the skew associated to the buffers and the local grid is identical for all the cases considered in this paper. Grid skew is the worst-case delay in the grid that distributes the clock signal to sequential elements (see Fig. 1), and is given in [14-15]. The skew caused by the buffers at the end of the H-tree, to which we will refer as buffer skew, was also calculated following the approach proposed in [15]. Contributions arising from variations of the following parameters are taken into account: threshold voltage, transistor channel length, gate oxide thickness, IR drop, and temperature non-uniformities.

(2) Global Skew

(a) Conventional and 3-D

There are two sources of global skew: the H-Tree, and repeater and buffer skews. The skew associated to the H-Tree is generated by ILD and wire thickness variations. For the repeaters and buffers, we considered the same skew contributions already mentioned above for buffers. However, because the size of the repeaters and buffers along the H-tree is smaller than that from one buffer, their skew, which typically scales with delay, is relatively small. Two extreme approaches are considered: one in which the dimensions of the interconnects that form the H-Tree are not scaled down with technology node, and another in which the interconnect dimensions are scaled down following the ITRS Roadmap. These two cases are considered because in real applications, the size of the H-Tree interconnects might be scaled down but not as aggressively as the lower metal layer interconnects. It is important to mention that inductance effects are ignored, and that this model considers the worst-case scenario in which all sources of skew add up at the same time. The clock distribution network for the 3-D technology uses the same process technology as the conventional; thus, it is reasonable to assume that all parameter variations are the same. The only differences are the halved die areas and the grids capacitance in the 3D structure.

(b) Optical

To compute waveguide-related skew, process variations including width, thickness, and material properties were considered. Since a 1% process variation introduces a 0.1% index variation, process variations in the waveguides typically contribute less than 0.4 ps of skew, which is relatively small compared to other skew sources. Detectors and trans-impedance amplifiers are the major contributions to global skew in an optical clock network. A total skew of 65 ps was reported for the detectors and amplifiers for the 0.18 μm node [16]. We will assume that the

trans-impedance delays will decrease at the same rate than the transistor delay (~ 0.7 per technology node). Since skew typically decreases with delay, it is reasonable to assume that the skew introduced by the detectors and trans-impedance amplifiers will also scale by 0.7 per generation.

(c) RF

The parameter variations in an RF H-Tree network are the same as in conventional technology. However, since the RF networks use wider metal lines for the H-Tree, parameters such as the resistance and capacitance differ from those in conventional circuits. Simulated resistance and capacitance values at different clock frequencies are used to calculate the global skew in the H-Tree. We used the amplifier skews reported in [12], which we scaled by 0.7 per technology node.

D. Clock Power

The total clock power dissipation can be divided into three parts: global clock power, buffer power, and local clock power. Similarly to the case of skew, buffer and local clock power will be the same for all technologies since their local clock distribution is identical. However, the global clock power of the different technologies will be different. Table II summarizes the parameters used in this section extracted from the 2001 ITRS.

(1) Buffer power and local clock power

The buffer power, P_{buffer} , and local clock power, P_{latch} , can be written as:

$$P_{\text{buffer}} + P_{\text{latch}} = (C_{\text{buffer}} + C_{\text{latch}}) \times V_{\text{dd}}^2 \times f$$

where C_{buffer} is the buffer capacitance and C_{latch} is the total capacitance of all the latches receiving the clock signal from a given grid. Here, the total buffer capacitance is related to the load capacitance of the latches and grid driven by it. For optimum delay-power trade-offs [17], the buffer capacitance is typically taken as:

$$C_{\text{buffer}} = 0.33 \times (C_{\text{latch}} + C_{\text{grid}})$$

The latch capacitance is defined as [17]:

$$C_{\text{latch}} = \left(\frac{1}{f_{\text{id}}} \right) \times W_{\text{avg}} \times N_{\text{tr}} \times C_{\text{trans}}$$

where f_{id} , the average logic depth, taken as 12 [19], N_{tr} is the number of transistors; W_{avg} is the average transistor size, and C_{trans} is the gate capacitance per unit length. The total grid capacitance for a 1-cm² chip was taken as 316 pF [4][18].

(2) Global power

(a) Conventional and 3-D

The power of the global clock distribution for the conventional case is given by,

$$P_{global} = (C_{H-Tree} + C_{repeaters}) \times V_{dd}^2 \times f_{global}$$

For 3-D, C_{H-Tree} and $C_{repeaters}$ are smaller. Therefore the global power of 3-D is smaller than conventional.

(b) Optical

Optical clock distribution uses light to deliver the clock signal via a waveguide-based H-tree. Assuming a value of 200 μ A for the output current of the detector [20], the detector power, $P_{detector}$, can be assessed by using the following equation:

$$P_{detector} = I_{detector} \times V_{dd}$$

Following Ref. [21], the amplifier power, $P_{amplifier}$, can be obtained from:

$$P_{amplifier} = I \times V_{dd} = \frac{1}{8} \left(\frac{W}{L} \right)^2 m_0 \frac{1}{W} \left(\frac{C}{W} \right) (V_{dd}^3)$$

(c) RF

The global dynamic power of consumed by the global RF clock distribution, P_{RF_H-Tree} is given by [12]:

$$P_{RF_H-Tree} = C_{H-Tree} \times V_{in_unit}^2 \times f$$

where V_{in_unit} is the minimum required voltage amplitude at the input of the clock tree that can provide sufficient power to the amplifier, which depends on frequency, and the attenuation constant of the interconnect [12]. The amplifier power of RF was taken equal to that of optical.

E. Metal-Layer Area Usage

The size of the H-Tree determines the global area usage. The total lengths of the H-Tree can be obtained and calculated following [19]. As mentioned before, two extreme approaches are considered: one in which the dimensions of the interconnects that form the H-Tree are not scaled down with technology node, and another in which the interconnect dimensions are scaled down following the ITRS Roadmap. The additional area used by shield lines that typically are added to protect clock lines from crosstalk was included. The width of the shield lines was taken equal to the width of the clock lines. For 3-D, the smaller die size lowers the area usage. This introduces the main difference from the conventional H-Tree area usage. The methodology and

other parameters for 3-D area usage calculation are the same as conventional.

For the optical technology, the waveguide size is maintained at $0.4\ \mu\text{m}$ for all technology nodes. Two scenarios are chosen here: one is that the waveguide layer is processed and treated as an additional layer; the other one is that the waveguide layer is integrated within the metal layer. Similarly, for RF, the widths of the H-Tree are not scaled. The parameters used for RF are based on the current technology.

III. RESULTS AND DISCUSSION

A. Clock Skew

The global clock skew versus year for conventional, 3-D, optical and RF clock distribution is shown in Fig. 3. The technology node and expected frequencies are also listed on this figure. In addition, for conventional clock distribution, as mentioned before, two cases are considered: one uses an H-Tree constructed with interconnects with dimensions that are scaled down by 0.7 with technology node; the other uses an H-Tree made with interconnects that are not scaled, i.e. their dimensions are those of the 130 nm node for all nodes.

It is clear that for scaled conventional, 3-D, and RF, global skew increases with technology node. However, in the cases of the non-scaled conventional and optical cases the global skew actually decreases with technology node. In the case of non-scaled conventional clock distribution, the decrease of skew with technology node results from the decreases of the dielectric constant and the improvement of the transistor speed expected by the ITRS. For the optical clock, the global skew decreases, mainly because of the assumption that the detector and trans-impedance amplifier will have a lower delay resulting in lower skew.

The global skew for the RF case increases because the impedance of the interconnect increases with frequency. For scaled conventional clock distribution, the significant increase of global clock skew with increasing frequency is partially caused by the increasing number of repeaters. On the other hand, for a non-scaled H-tree structure, the global skew is almost constant and smaller than that of the other clock-distribution technologies. For the 3-D case, the skew is lower than that of the corresponding conventional case because the die size is considerably smaller. In summary, optical and RF have better performance at very high frequencies compared to the conventional case with an aggressively scaled H-Tree. However, if the H-Tree is not scaled down, the global clock skew is found to be below 5 ps, which is difficult to improve with alternative technologies.

To obtain total clock skew, the contributions of the buffers and local clock distribution are added to the global skew. Fig. 4 shows the calculated total clock skew versus technology node for the different clock distribution alternatives. This figure

shows that the total clock skew increases with frequency (and frequency node). The buffer and local skew contribute the majority of the total clock skew at high frequency. For the case of scaled Cu interconnects, skew increases monotonically. On the other hand, for non-scaled Cu interconnects, the skew decreases due to the benefits resulting from a relative aggressive dielectric constant reduction, which slows down after the 65 nm node. The relative abrupt change at the 65 nm node results from a 30% decrease of supply voltage predicted by the 2001 ITRS. A significant research effort is being made on investigating alternative interconnects for global clock distribution, with the goal of decreasing the total clock skew by reducing the global clock skew. However, the results of this study suggest that to reduce total clock skew, improvements at the local level of clock distribution should be made. Moreover, we have found that just by not scaling down the dimensions of the H-tree, relatively low skews are achieved.

As frequencies increase, the budgets for clock skew reduce, ideally as the inverse of the frequency. Consequently, a constant skew as a function of technology node is equivalent to a decrease in clock distribution performance. For guidance, we have included in Fig 4 a curve representing 20 % of the clock period. It can be observed that in all cases, the total skew will surpass the 20 % curve around the 65 nm node according to our estimations.

It is interesting to note that by increasing the level (n) of the H-Tree, the buffer size (and skew) can be decreased, since the total number of transistors in each local area or grid decreases. Unfortunately, balancing H-trees with many levels is difficult from a practical point of view. In addition, the number of repeaters in the H-tree increases, which partially offsets the gain of increasing n. Finally, increasing n also results in an increasing number of neighboring sequential elements with large timing differences, which is very detrimental for chip performance.

Figure 5 shows the relative amounts of skew contributions from different sources in a 10-level H-Tree using scaled conventional clock distribution at 2.3 and 28.8 GHz. At 2.3 GHz, the global contribution (H-Tree, and repeaters and buffers) is 41% of the total clock skew, and reaches 44% at 28.8 GHz. For the non-scaled conventional clock distribution, global skew plays an important role at very high frequencies. Figure 6 compares the global skew with and without scaling at 28.8 GHz, and shows that with scaling the global skew is 37% of the total skew, but it is only 9% for the non-scaled case.

B. Clock Power

Figure 7 shows the total clock power of the different clock distribution technologies as a function of technology node and frequency. The total microprocessor power predicted by ITRS is also shown for reference. Figure 7 shows

that at high frequencies, the clock power for different technologies is almost the same. This is a consequence of the fact that the power from the global distribution of all interconnect technologies is significantly lower than the power consumption of the buffers and the local clock distribution. Therefore, the interconnect technology used for global distribution is of little consequence in terms of power. Figure 7 also shows the total power of a Pentium 4 operating at 2.53 GHz (58 W), which is significantly lower than the prediction of the ITRS 2001.

It is also interesting to note that the ratio between our estimated clock power for conventional interconnects and the total microprocessor power predicted by the ITRS is approximately constant at 25 %. In other words, as expected, our estimations for clock power increase at approximately the same rate than the total microprocessor power predicted by the ITRS. The increase of clock power is partly mitigated by the expected decrease in V_{DD} .

The power density of all interconnect technologies is shown in Fig. 8. 3-D has the highest power density because of the smaller die area. This high power density could create challenges for power extraction in some applications.

C. Area Usage

Figure 9 shows the calculated metal layer area used for global distribution for different interconnect technologies. An H-Tree with 8 levels is used in all technologies. For conventional and 3-D technologies, aggressively scaled H-Tree structures are used. For optical, two cases are considered. The first case uses a waveguide that is integrated with the top metal layer; the other case uses a waveguide implemented in an additional dielectric layer. Therefore, for the second case, the waveguide layer will be treated as a half layer because a metal layer and a dielectric layer together count for one layer. Except for optical (with the additional layer), all the area usages are smaller than 4%. This is a relatively small number and indicates that the top layer usage is not very large for all interconnect technologies.

IV. CONCLUSIONS

Our simple comparison of the performance of alternative clock distributions that utilize scaled and non-scaled conventional Cu interconnects, 3-D, RF and optical interconnects revealed the relative importance of the contributions to skew and power. The numerical values were obtained from the 2001 ITRS, and a common metrics was used to benchmark the different alternatives. For global clock skew, 3-D exhibits a better performance than conventional because of the smaller die size. Our results also suggest that RF and optical may have advantages at very high frequencies, above 30

GHz. Simple extension of conventional clock distribution in which the interconnects used for clock distribution are scaled down shows that skew increases in absolute terms with frequency, which compounded with reducing skew budgets for skew, has detrimental effects on chip performance. However, if the interconnects are not scaled, the skew slightly decreases with technology node. This analysis also indicates that the fraction of skew contributed by global clock distribution is a small fraction of the total skew, and that most skew is generated at the buffer and local network. Similarly, most power is consumed by the buffers and local distribution network. Consequently, replacing or improving the global clock distribution is not expected to substantially decrease total clock skew and power.

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FIGURE AND TABLE CAPTIONS

Figure 1: A buffered H-tree clock distribution network with four levels ($n = 4$).

Figure 2: Schematic diagrams of the alternative clock distributions.

Figure 3: Global clock skew versus year for conventional, 3-D, optical and RF clock distribution.

Figure 4: Total clock skew versus technology node for the different clock distribution alternatives.

Figure 5: Relative amounts of skew for different sources in a 10-level H-Tree using a conventional technology with scaling at 2.3 and 28.8 GHz.

Figure 6: Comparison the global skew with and without scaling at 28 GHz.

Figure 7: Total clock power of the different clock distribution technologies as a function of technology node and frequency.

Figure 8: Power density of different interconnect technologies.

Figure 9: Metal layer area used for global distribution for different interconnect technologies.

Table 1: Components for each interconnect technology.

Table 2: Important parameters used for power calculation.

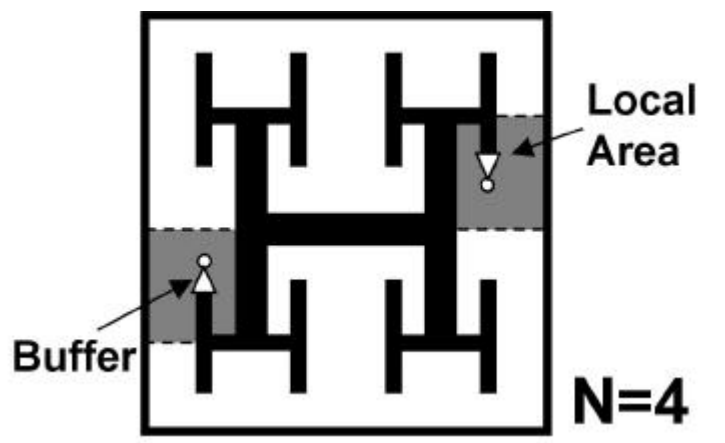
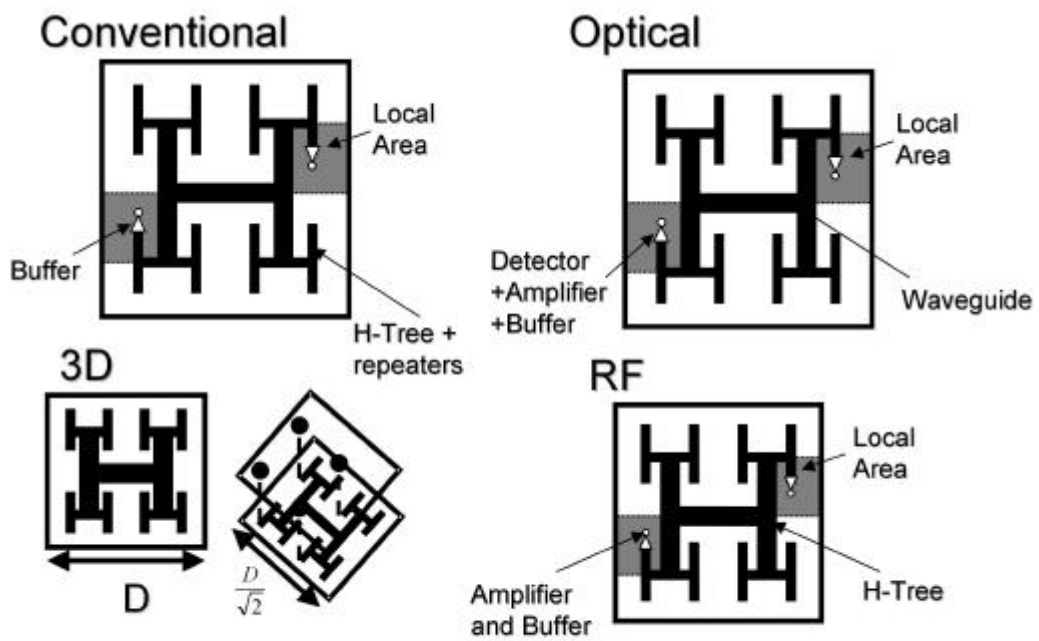


Figure 1 A buffered H-tree clock distribution network with four levels ($n = 4$)



All technologies use electrical clock distribution in local area.

Figure 2 Schematic diagrams of the alternative clock distributions

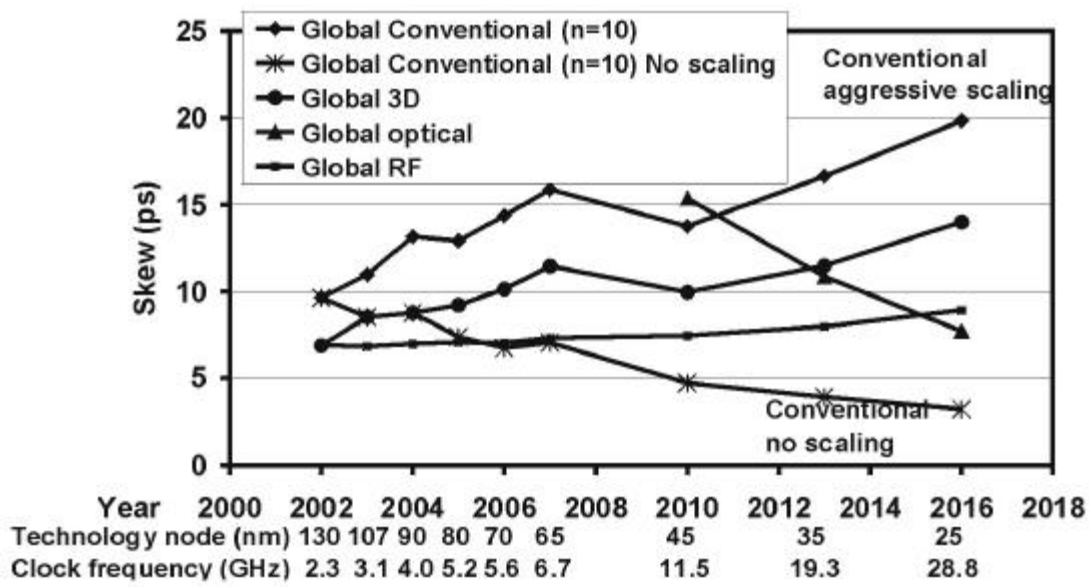


Figure 3 Global clock skew versus year for conventional, 3-D, optical and RF clock distribution

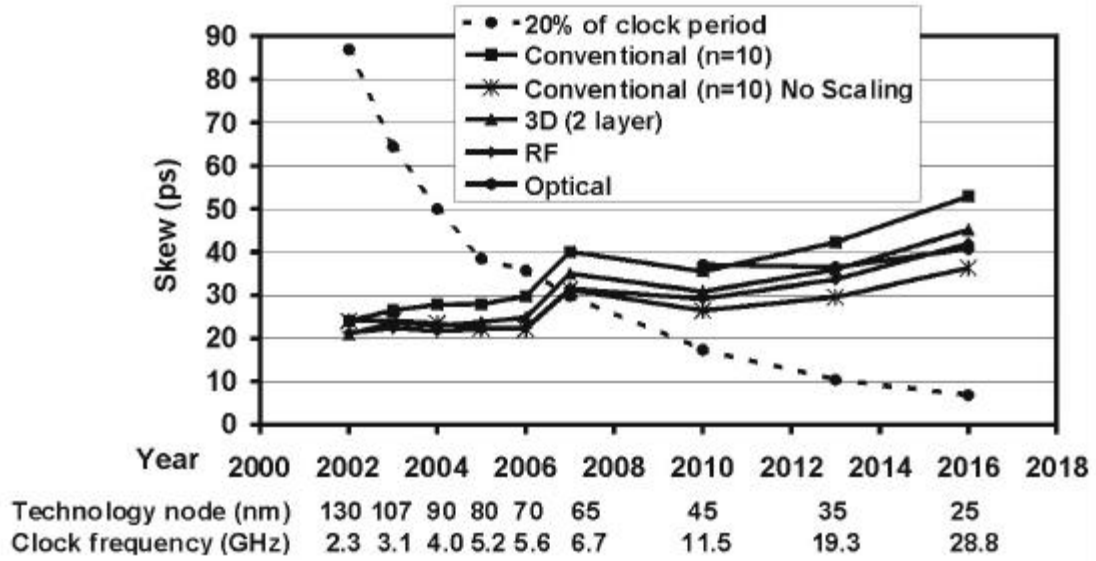


Figure 4 Total clock skew versus technology node for the different clock distribution alternatives

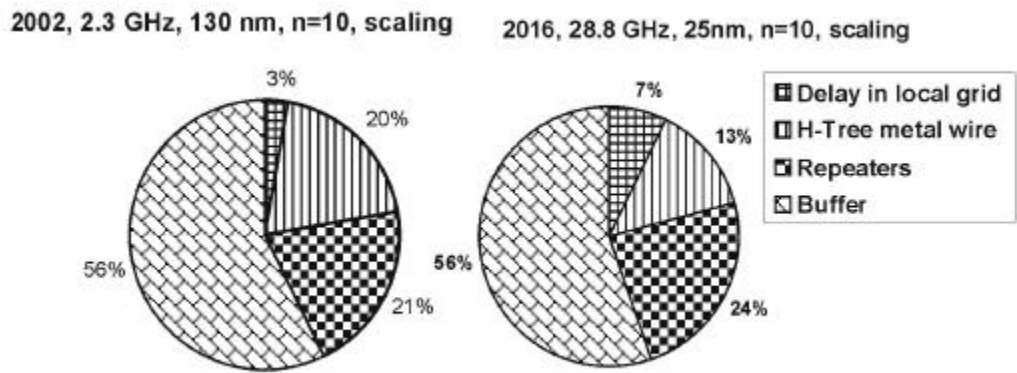


Figure 5 Relative amounts of skew for different sources in a 10-level H-Tree using a conventional technology with scaling at 2.3 and 28.8 GHz

2016, 28.8 GHz, 25 nm, n=10, no scaling 2016, 28.8 GHz, 25nm, n=10, scaling

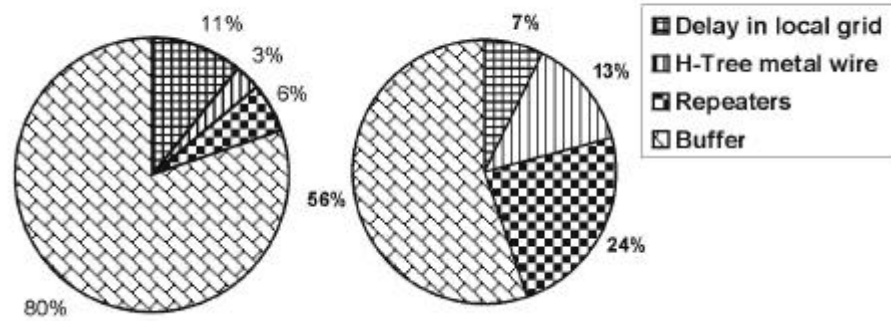


Figure 6 Comparison the global skew with and without scaling at 28.8 GHz

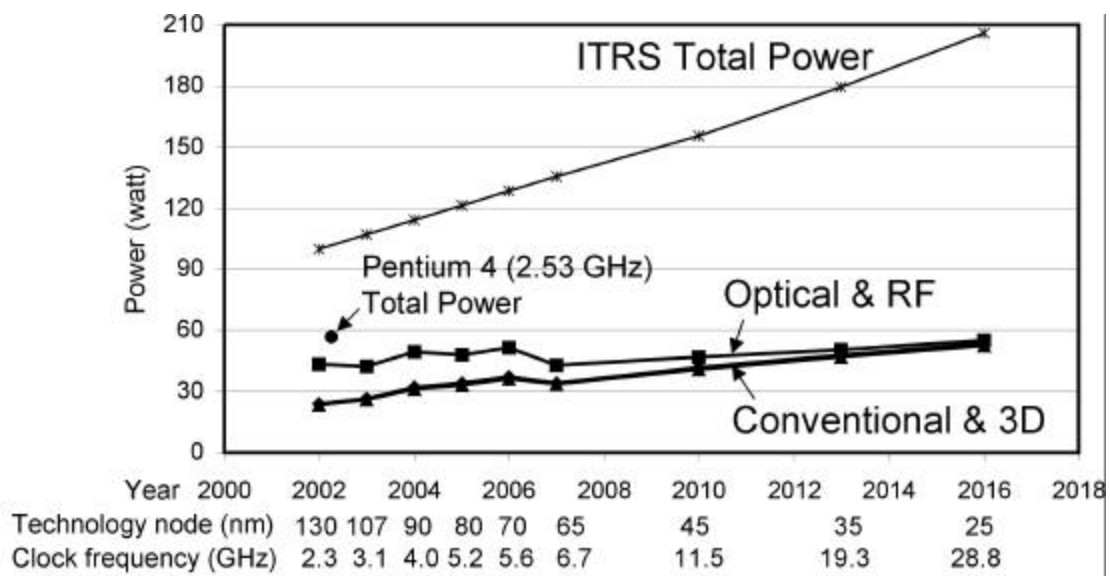


Figure 7 Total clock power of the different clock distribution technologies as a function of technology node and frequency

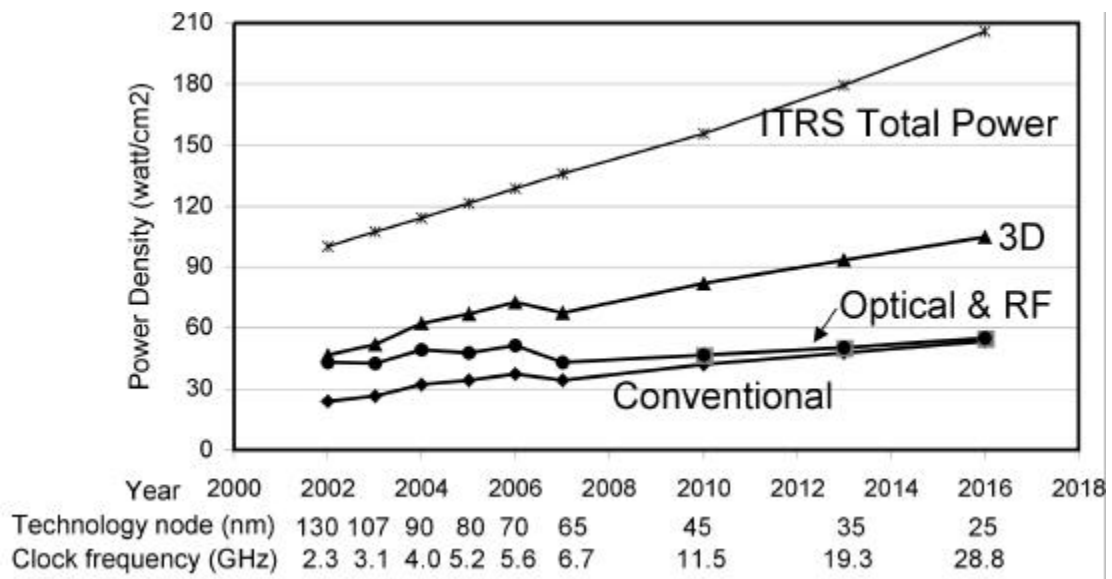


Figure 8 Power density of different interconnect technologies

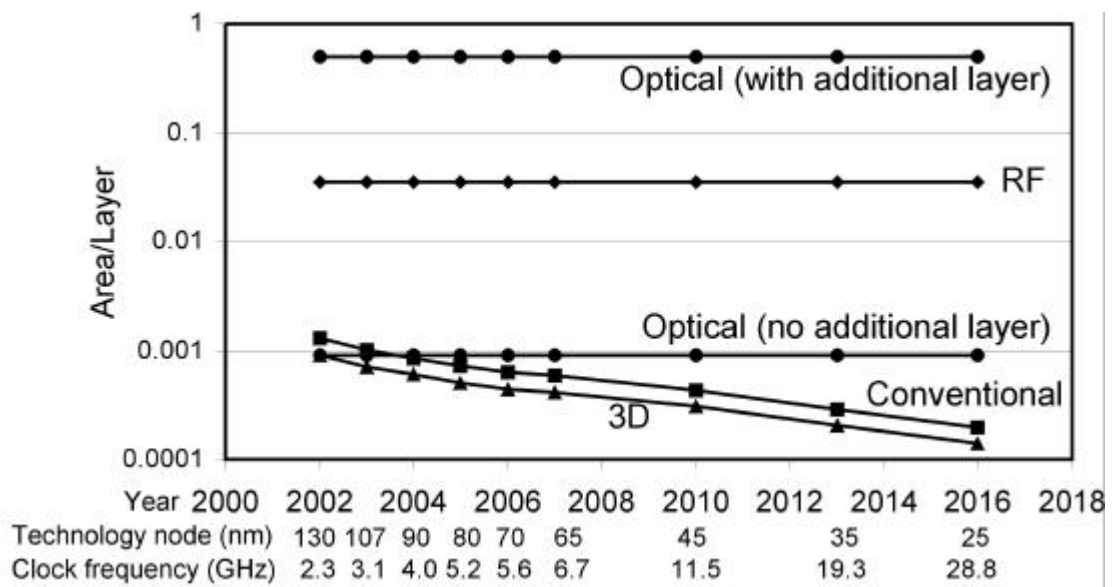


Figure 9 Metal layer area used for global distribution for different interconnect technologies

		Global ←		→ Local	
Conventional	H-Tree	Repeaters		Buffer	Grids + Latches
Optical	H-Tree		Detectors+ Amplifiers	Buffer	Grids + Latches
RF	H-Tree		Amplifiers	Buffer	Grids + Latches
3D	H-Tree	Repeaters		Buffer	Grids + Latches

Table 1 Components for each interconnect technology

V_{dd}	Supply Voltage
f	Clock frequency
f_{ld}	Average logic depth
W_{avg}	Average transistor size
N_{tr}	Number of transistors
C_{trans}	Gate capacitance per unit length
V_{in_unit}	Minimum required voltage at the input of clock tree

Table 2: Important parameters used for power calculation.