Low-Voltage Comparator-Based Switched-Capacitor Sigma-Delta ADC

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Many analog signal processing circuits use operational amplifiers (op-amps) in a negative feedback topology. Error in these feedback systems is inversely proportional to the gain of the op-amp. Because scaled CMOS technologies use smaller channel lengths and require lower power supply voltages, it becomes more difficult to implement high gain op-amps. Recently, a comparator-based switched-capacitor (CBSC) technique was proposed [1] that uses a comparator rather than an op-amp to implement switched-capacitor topologies. One of the biggest challenges of low voltage circuits is the transmission gates that must pass the signal. If the signal is near the middle of the power supply range, neither the NMOS nor the PMOS transistor has sufficient gate drive to pass the signal properly. The switched-op-amp technique [2] was proposed to mitigate this problem. In this technique, the output of the op-amp is directly connected to the next sampling capacitor without a transmission gate. During the charge transfer phase, the op-amp is switched off, and the output is grounded. Much like the standard switched-capacitor technique, CBSC circuits use two-phase clocking, having both sampling and evaluation clock phases. Unlike a standard switched-capacitor circuit, in a CBSC circuit all current sources connected to the output node are off at the end of the evaluation phase. Thus, the CBSC technique is inherently better suited to low-voltage applications than switched-op-amp circuit topologies. Although the previous CBSC implementation was a single-ended version, many high-resolution systems require fully differential implementation for better power supply and substrate noise rejection properties. Since the CBSC is a new technique without an op-amp, existing fully differential circuitry cannot be applied. In this program, we are developing fully-differential CBSC topologies for applications in high resolution data conversion. Figure 1 shows a fully-differential low-voltage CBSC integrator stage using the combined techniques. We recently designed a fourth-order sigma-delta ADC for operation at 1-V power supply using this integrator stage.

![Figure 1: Fully-differential comparator-based switched-capacitor integrator. The input of the next integrator stage is also shown. Common-mode feedback circuits are not shown.](image)

**REFERENCES**
