Comparator-based Switched-capacitor Circuits (CBSC)
J.K. Fiorenza, T. Sepke, P. Holloway, H.-S. Lee, C.G. Sodini
Sponsorship: MARCO C2S2, CICS

Two side effects of technology scaling that have a significant impact on analog circuit design are the reduced signal swing and the decrease in intrinsic device gain. Gain is important in feedback-based, analog signal processing systems because it determines the accuracy of the output value. Cascoded amplifier stages have been a popular solution to increase amplifier gain, but they further reduce the signal swings of scaled technologies. An alternative method for achieving high gain in an operational amplifier without reducing signal swing is to cascade several lower gain amplifiers. Nested-Miller compensation approaches can be used to stabilize the cascaded feedback system, but the frequency response of the closed loop system is significantly sacrificed to ensure stability. In this project [1-2], we explore a new comparator based switched capacitor (CBSC) circuit design methodology that eliminates the use of op-amps in sampled data systems.

A sampled-data system typically operates in two phases, a sampling phase (φ1) and a charge transfer phase (φ2). An important property of these systems is that the output voltage needs to be accurate only at the moment the output is sampled. No constraint is placed on how the stage gets to the final output value. Feedback systems use a high-gain operational amplifier to force a virtual ground condition at the op-amp input. The top circuit in Figure 1a shows the conventional op-amp-based switched-capacitor gain stage. The circuit in Figure 1b shows the proposed CBSC approach, where a comparator and a current source have replaced the op-amp. Assuming the comparator input v_X starts below the common-mode voltage at v_CM, the current source charges the output circuit until the comparator detects the virtual ground condition and turns the current source off. At this instant, the output is sampled on C_L. Because the CBSC design ensures the same virtual ground condition as the op-amp based design, both circuits produce the same output value at the sampling instant. This property of the CBSC technique is demonstrated by the waveforms for the two circuits shown in Figure 2.

The CBSC concept is general and can be applied to any sampled-data analog circuit. For example, the CBSC design approach can be applied to a pipelined ADC. A prototype 1.5-b/stage CBSC pipeline ADC was constructed and operates similarly to the op-amp version of the ADC. The prototype CBSC ADC was implemented in a 0.18-µm CMOS technology. The active die area of the ADC is 1.2 mm². At a 7.9 MHz sampling frequency, the DNL is +0.33/-0.28 LSB, and the INL is +1.59/-1.13 LSB. Its ADC achieves an SFDR of 62 dB, an SNDR of 53 dB, and an ENOB of 8.7 b for input frequencies up to the Nyquist rate. The core ADC power consumption of all 10 stages of the pipeline converter is 2.5mW at a 1.8V power supply, resulting in a 0.8 pJ/b figure of merit.

References