Problems/Issues with most $D_{it}$ characterization techniques

- $C_{ox}$ hard to extract – maximum capacitance can exceed $C_{ox}$ (border traps)
- Energy range limitations, specially inside bands
- Separation of inversion response
- Capture cross section determination
- Border traps vs. interface states?
- Limited knowledge of semiconductor band structure
- Sensitivity to other factors (doping level, etc)
- Large uncertainty (~4x at best?)
- Unclear applicability to quantum-well structures
Best techniques seem to be combinations

- Penn State admittance technique (equivalent circuit model of G-V and C-V vs f)
- Sematech combination of low-f/high-f low-T/high-T + conductance + Terman
- IMEC full conductance technique at different T
- Albany Hall+C-V technique
- Charge pumping technique
- Use highest possible f
- All must include detailed self-consistent P-S simulations of C-V characteristics
- Subthreshold swing in transistors yet to be exploited
- Should be doing thorough error analysis (as IMEC)
Wrap up

• Thanks to Ted Equi for dealing with all the logistics
• Thanks to speakers for preparing these talks
• Thanks to our sponsors, the FCRP program, for suggesting and supporting the organization of this workshop
• All materials will be available online shortly.